UCA32 Global Register Reference Manual

Publication No. 1500-096 Rev. 1.31

Firmware Rev. 6.09

Supporting Products:

- QPCX-1553
- RAR15-XMC
- RXMC-1553
- R15-MPCIE
- QCP-1553
- RPCIe-1553
- RXMC2-1553
- R15-USB-MON
- R15-LPCIE
- QPM-1553
- R15-PMC
- R15-EC
- Q104-1553P
- R15-USB

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Document History

Revision	Date	Description
1.31	July 19, 2017	Added R15-USB-MON to product list.
1.30	November 8, 2016	Extended the Global Register region past 0xFF to 0x1FF to make room for ADC conversions. Added support for the R15-MPCIE. Corrected Upper Time Tag words for ttcl and ttc from [63:48] to [63:32]. Rebranded to Abaco Systems.
1.28	March 24, 2016	For RT Offsets for Channels 1-4, Dbl Wd 0x02, bit [4:0] definition, changed “OFFSET_EN” to “ADD_BASE”.
1.27	November 18, 2014	Updated our new address, the firmware revision from 6.00 to 6.05 and the products supported on the front page.
1.26	November 8, 2013	Updated temp sensor portion.
1.25	April 1, 2013	Added comments that when an RS485 channel is used as a trigger output, the associated TXEN must be enabled.
1.24	February 14, 2013	Added board types to CSC Control Register and changed FPGA Revision to generic 32 bits.
1.23	January 18, 2013	Added the PIO interface registers and added PIO functionality to the trigger control registers.
1.22	January 15, 2013	In Dbl Wd 0x36, for bit 12, changed from “Set per the table below” to " Set per the table above”.
1.21	December 4, 2012	Added notes to discretes, differentials and triggers that the trigger function is ORed with the respective output which allows for manual testing of the trigger.
1.20	August 7, 2012	Added discrete and differential option registers. Added a bit in the trigger input and output control registers which reports whether a dedicated trigger input/output is available. Added additional temp sensor interface info.
1.10	June 27, 2012	Changed DW 0x27 from Board Status to System Reset control.
1.00	May 8, 2012	Initial release.

Waste Electrical and Electronic Equipment (WEEE) Returns

Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

About This Manual

Conventions

Notices

This manual may use the following types of notice:

WARNING

Warnings alert you to the risk of severe personal injury.

CAUTION

Cautions alert you to system danger or loss of data.

NOTE

Notes call attention to important features or instructions.

TIP

Tips give guidance on procedures that may be tackled in a number of ways.

LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Definitions

The following terms are used throughout this document and are defined as follows unless noted otherwise:

- Set: Read or Write a logic one (“1”)
- Clear: Read or Write a logic zero (“0”)

Further Information

Abaco Website

You can find information regarding Abaco products on the following website:

LINK
https://www.abaco.com

Abaco Documents

This document and other reference documentation is distributed via the Abaco website. You may register for access to manuals via the website.

LINK
https://www.abaco.com/products/avionics

Third-party Documents

NOTE
Technical literature describing components used on the MIL-STD-1553 products is available from the manufacturers' websites.

Technical Support Contact Information

You can find technical assistance contact details on the website Embedded Support page.

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https://www.abaco.com/embedded-support

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:

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support@abaco.com

Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.

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Do not return products without first contacting the Abaco Repairs facility.

Contents

List of Tables

1 • Introduction

This document describes the Memory Map and Global Registers used with Abaco Systems' Enhanced Universal Core Architecture (herein called UCA32) for MIL-STD-1553 products.

UCA32 provides evolutionary changes to our existing Universal Core Architecture (UCA) which includes the following:

- UCA Engine upgraded to 32-bit processor
- All registers and pointers now 32 bits
- Time Tags are now 64 bits with 1-ns resolution
- BC/RT/BM control enhancements
- Control registers modified to be "thread-safe"
- Memory map modified to be multiple-partition friendly

Although UCA32 has resulted in many low-level changes, the API makes a lot of those changes seamless.

The UCA32 architecture is used on the products listed on the title page of this document and is primarily intended to be incorporated on Abaco's newest products. However, should you have an interest in UCA32 for a product not listed on the title page, contact Abaco's Technical Support via the link below.

LINK

support@abaco.com

This document is primarily for those who do not wish to use the API library and intend to write their own low-level driver. This Core Architecture is the low-level hardware interface that is common to many of Abaco's MIL-STD-1553 boards. Provided with these products is an easy-to-use, high-level programmer's library called BusTools/1553-API. This library is a software layer, written on top of UCA/UCA32. For a description of the API usage, see the "BusTools1553-API Software User Manual". For a hardware description, see the "MIL-STD-1553 Hardware Installation and Reference Manual". For details regarding the individual control of each 1553 channel or LPU (Local Processing Unit) as it is referred, please see the "MIL-STD-1553 Enhanced Universal Core Architecture (UCA32) Local Processing Unit (LPU) Reference Manual".

2 • Memory Map

Table 2-1 below provides the memory map for UCA32. The memory is partitioned so that the global registers are grouped together in comparison to the 1553 channel control registers which are grouped by channel. The File Registers for each 1553 channel are described in the UCA32 Local Processing Unit (LPU) Reference Manual. The remaining registers are defined in this document.

Table 2-1 UCA32 Board Memory Map

Function	Double Word Offset lb_a[22:2]		Byte Offset lb_a[22:0]	
	Start	End	Start	End
GLOBAL REGISTERS	0x0	0x1FF	0x0	0x7FF
DMA Control Registers	0x3000	0x30FF	0xC000	0xC3FF
SMP LOCK REGISTERS				
4K dbl wd x 1	4000	4FFF	0x10000	0x13FFF
Reserved (4K dbl wd x 1)	5000	5FFF	0x14000	0x17FFF
SHARED MEMORY	8000	83FF	0x20000	0x20FFF
CH1				
File Registers	C000	C0FF	0x30000	0x303FF
Time Tag Registers	C400	C405	0x31000	0x31017
Triggers	C800	C801	0x32000	0x32007
CH2				
File Registers	D000	D0FF	0x34000	0x343FF
Time Tag Registers	D400	D405	0x35000	0x35017
Triggers	D800	D801	0x36000	0x36007
CH3				
File Registers	E000	E0FF	0x38000	0x383FF
Time Tag Registers	E400	E405	0x39000	0x39017
Triggers	E800	E801	0x3A000	0x3A007
CH4				
File Registers	F000	F0FF	0x3C000	0x3C3FF
Time Tag Registers	F400	F405	0x3D000	0x3D017
Triggers	F800	F801	0x3E000	0x3E007

Function	Double Word Offset lb_a[22:2]		Byte Offset lb_a[22:0]	
	Start	End	Start	End
Reserved for ARINC on multi-protocol boards[1]	0x40000	0x5FFFF	0x100000	0x17FFFF
RAM MEMORY	100000	1CFFFF	400000[2]	7FFFFF[3]
e.g. CH 1	100000	13FFFF	400000	4FFFFF
e.g. CH 2	140000	17FFFF	500000	5FFFFF
e.g. CH 3	180000	1BFFFF	600000	6FFFFF
e.g. CH 4	1C0000	1CFFFF	700000	7FFFFF

[1] For multiple-protocol boards, this region is reserved for ARINC functionality.
[2] The starting address of user RAM is hard coded in the FPGA and presented at DW 0x22 as “User RAM Start Location”. If the board has 4 MBytes (1 M DW) of RAM, this starting address would also be 4 MBytes (1 DW).
[3] The ending address of user RAM can be determined by the starting address identified in Footnote 2 and the amount of RAM installed on the board, hard coded in the FPGA and provided at DW 0x23 as “User RAM Amount”. If the board has 4 MByte (1 M DW) of RAM, the ending address would be 8 MBytes (2 M DWs).

3 • Global Registers

This chapter describes the Global Registers. A memory map of the global registers is shown below with the various registers divided into sections. Following the memory map are the individual register descriptions in sequential memory order. The Enable (decimal) column in the memory map is a reference for internal use only.

3.1 Global Register Summary

Table 3-1 Global Register Summary

Register	Read/ Write	Double Word Offset	Byte Offset	Enable (Decimal)
Generic Configuration Data Mirrored from Flash				
CSC	R/W	0x00	0x00	0
Board Specific	R	0x01	0x04	1
RT Offsets Ch 1 – 4	R	0x02	0x08	2
RT Offsets Ch 5 - 8	R	0x03	0x0C	3
Options Ch1	R	0x04	0x10	4
Options Ch2	R	0x05	0x14	5
Options Ch3	R	0x06	0x18	6
Options Ch4	R	0x07	0x1C	7
Options Ch5	R	0x08	0x20	8
Options Ch6	R	0x09	0x24	9
Options Ch7	R	0x0A	0x28	10
Options Ch8	R	0x0B	0x2C	11
Board S/N	R	0x0C	0x30	12
Discrete Options	R	0x0D	0x34	13
Differential Options	R	0x0E	0x38	14
PIO Options	R	0x0F	0x3C	15
Not used	R	0x10 – 1F		
Board				
FPGA Rev	R	0x20	0x80	32
Interrupt Status all devices	R	0x21	0x84	33
User RAM Start Location	R	0x22	0x88	34
User RAM Amount	R	0x23	0x8C	35
LED Control	W	0x24	0x90	36
Temp Sensor Read Cmd	R/W	0x25	0x94	37

Register	Read/ Write	Double Word Offset	Byte Offset	Enable (Decimal)
Temp Sensor Write Cmd	W	0x26	0x98	38
System Reset Control	R/W	0x27	0x9C	39
Not used		0x28 – 2F		
I/O				
Discrete Out	R/W	0x30	0xC0	48
Discrete In	R	0x31	0xC4	49
RS485 Transmit & Control	R/W	0x32	0xC8	50
RS485 Data	R	0x33	0xCC	51
Ext RT Address	R	0x34	0xD0	52
Reserved		0x35	0xD4	53
DAC Control	W	0x36	0xD8	54
PIO Control	R/W	0x37	0xDC	55
Not used		0x38 – 4F		
Timing				
IRIG Control	R/W	0x50	0x140	80
IRIG TOY	W	0x51	0x144	81
Reset All Time Tag Registers	W	0x52	0x148	82
Not used		0x53 – 5F		
Reserved				
Reserved for System Use		0xA0 – AF	0x280 – 2BF	160 – 175
FPGA Analog-to-Digital Converter (ADC)				
FPGA Die Temp	R	0x100	0x400	256
FPGA Vccint	R	0x101	0x404	257
FPGA Vccaux	R	0x102	0x408	258
FPGA ADC Vp/Vn	R	0x103	0x40C	259
FPGA Vccbram	R	0x106	0x418	262

3.2 Global Register Descriptions

3.2.1 Generic Configuration Data Mirrored from Flash (Dbl Wd 0x00 – 0x1F, Bytes 0x00 – 0x7C)

Upon power-up or a software reset, various flash locations dedicated to a board's configuration is read and mirrored here. All the registers here are read-only except for the software reset function available in the CSC Control Register. There are some features however that the user can program with a flash programmer like the RT Offset registers.

The RT Offset registers allow the user to predefine an individual 1553 channel's RT Address as either being an offset to an external hardwired RT Address if available or to act as a hard-coded RT Address.

CSC Control Register (Dbl Wd 0x00, Bytes 0x00 – 0x03)

The Control/Status Configuration (CSC) Register is used to identify, configure and reset the board.

Table 3-2 Control/Status Configuration Read Register

Bit	Field	Definition	
0	0x0	Clear	
5-1	bd_type	Board Type These bits identify the board base model in the embedded table below.	
		BD_TYPE	Board Base Model
		0	Unassigned
		1	QPM
		2	N/A[4]
		3	QPCX
		4	N/A
		5	Q104P
		6	N/A
		7	QcP
		8	N/A
		9	R15-EC
		10	N/A
		11	RXMC-1553
		12	RPCIe
		13	Unassigned
		14	RXMC2

[4] "N/A" indicates a legacy product not supported by UCA32.

Bit	Field	Definition	
		15	R15-LPCIe
		16	USB-1553
		17	RAR15XMC
		18	RAR15XMC-XT
		19	R15-PMC
		20	R15-MPCIE
10-6	ch_num	Channel Number Directly identifies the number of 1553 channels supported. If the value is 1, then one 1553 channel is supported. If the value is 2, then two 1553 channels are supported, etc.	
11	mode	Mode If clear, all 1553 channels support dual-mode. If set, all 1553 channels support multi-mode. Dual-mode boards offer a bus monitor (BM) capability in addition to either multiple Remote Terminals (RT) or Bus Controller (BC) capability. Multi-mode boards provide for simultaneous BC, BM and RT operation.	
12	irig	IRIG	
13	0x0	Clear	
14	uca32	Set if UCA32 firmware is used. Clear if UCA firmware is used.	
15	0x1	Set	
18-16	Reserved		
19	vv	1553 Variable Voltage If set, indicates variable-voltage 1553 transceivers are provided for all channels. If cleared, variable voltage is not provided or enabled.	
20	btest	Bus Tester If clear, then Channel 1 is a Bus Tester for extended error injection and RT validation testing. If set, then Channel 1 cannot be a Bus Tester.	
24-21	Reserved		
25	wp	Flash Write Protect If clear, then the flash is write protected and cannot be written to and must be returned to the factory should the user want to program flash. When set, flash is not write protected which is the default.	
30-26	Reserved		
31	0x0	Clear	

Table 3-3 Control/Status Configuration Write Register

Bit	Field	Definition
0	sw_rst	Software Reset Setting this bit resets all logic and registers on the board. This bit cannot be read back.
31-1	N/A	Not Used

Board Specific Register (Dbl Wd 0x01, Bytes 0x04 – 0x07)

The Board Specific Register can further extend the board functionality for each specific board model. If a board is not listed here, the register is not used and undefined.

Table 3-4 RAR15-XMC Board Specifics (Read Only)

Bit	Field	Definition
0	P1	P1 Front I/O connector. Set if installed; clear if not installed.
1	P14	P14 Rear I/O Connector. Set if installed; clear if not installed.
2	P16	P16 Rear I/O Connector. Set if installed; clear if not installed.
31-3	Reserved	

Table 3-5 RAR15-XMC-XT Board Specifics (Read Only)

Bit	Field	Definition
0	P1	P1 Front I/O connector. Set if installed, clear if not installed.
1	P14	P14 Rear I/O Connector. Set if installed, clear if not installed.
2	P16	P16 Rear I/O Connector. Set if installed, clear if not installed.
31-3	Reserved	

RT Offsets for Channels 1-4 (Dbl Wd 0x02, Bytes 0x08 – 0x0B)

The hardwired RT address offsets for 1553 channels 1 – 4 are user-modifiable on a channel-per-channel basis in flash and can be reviewed in Table 3-6.

RT Offsets for Channels 5-8 (Dbl Wd 0x03, Bytes 0x0C – 0x0F)

This register is reserved for hardwired RT address offsets for 1553 channels 5 – 8 if they exist. The bit definitions are listed in Table 3-6, replacing channels 1-4 with 5-8, respectively.

Table 3-6 RT Address Offsets for 1553 Channels 1 – 4 (Read Only)

Bit	Field	Definition
4-0	Offset_ch1	RT Offset Address Default = 0 for all channels. Functions as either an offset value applied to an external RT Address or as the channel's hardware RT address itself (depending on the value of ADD_BASE bit**).** User must take care not to program values that result in an invalid RT address (i.e. 31 in MIL-STD-1553B). Default = 0 for all channels
5	1760n_ch1	Enable 1760 Response Not When cleared (the default), 1760 startup response for the channel is enabled. When set, 1760 startup response for the channel is disabled.
6	add_base_ch1	Add Base Offset When set (default), the hardware RT address for the channel is the offset plus the external RT address. Parity is inherited from the external RT address and must be correct for the 1553 channel to use the combined RT address. When

Bit	Field	Definition
		cleared, the offset value is used as the hardware RT address for the channel with correct parity being passed to the 1553 channel.
7	Reserved	
12-8	Offset_ch2	See offset_ch1 above.
13	1760n_ch2	See 1760n_ch1 above.
14	add_base_ch2	See add_base_ch1 above.
15	Reserved	
20-16	Offset_ch3	See offset_ch1 above.
21	1760n_ch3	See 1760n_ch1 above.
22	add_base_ch3	See add_base_ch1 above.
23	Reserved	
28-24	Offset_ch4	See offset_ch1 above.
29	1760n_ch4	See 1760n_ch1 above.
30	add_base_ch4	See add_base_ch1 above.
31	Reserved	

Channel-Specific Configuration Options, Channels 1 - 8 (Dbl Wd 0x04– 0x0B, Bytes 0x10 – 0x2F)

The channel-specific configuration options are user-modifiable on a channel-per-channel basis in flash and define how the specific channel behaves upon power-up.

NOTE

Some boards have the 1553 outputs hardwired as transformer or direct coupled, so in that case, the XC_DC bit would have no meaning.

The channel-specific configuration options for channels 1 – 8 (listed in Table 3-8) are identical for all channels. See Table 3-7 for the address used by each channel.

Table 3-7 Double Word for Channels 1 – 8

Channel	Dbl Wd	Byte Offset	Channel	Dbl Wd	Byte Offset
1	0x04	0x10 – 0x13	5	0x08	0x20 – 0x23
2	0x05	0x14 – 0x17	6	0x09	0x24 – 0x27
3	0x06	0x18 – 0x1B	7	0x0A	0x28 – 0x2B
4	0x07	0x1C – 0x1F	8	0x0B	0x2C – 0x2F

Table 3-8 Channel-Specific Configuration Options, Channels 1 - 8 (Read Only)

Bit	Field	Definition
0	bm_only	BM Only When set (default), channel may function as BM, RT or BC. When cleared, channel may only function as BM.

Bit	Field	Definition
1	xcdc	Transformer coupled/Direct coupled Set defines transformer coupling (long stub) and cleared defines direct coupling (short stub).
2	b_a	1553 A or B Set defines 1553B and cleared defines 1553A.
3	rtvaln	RT Validated When set, channel has multi-RT, BC and BM functionality as programmed by the *mode* bit in the CSC. When cleared, channel functions as a single validated RT and as a BM. The *mode* bit in the CSC is ignored
31-4	Reserved	

Board S/N Register (Dbl Wd 0x0C, Bytes 0x30 – 0x33)

This register provides the board serial number if supported by the board. A value of 0x0 indicates that the serial number is not supported.

Table 3-9 Board Serial Number Register (Read Only)

Bit	Field	Definition
31-0	ser_no	Board Serial Number

Discrete Options Register (Dbl Wd 0x0D, Bytes 0x34 – 0x37)

This register provides a bit for each potential discrete I/O (up to 31). A bit value of 0 indicates that the discrete I/O is not supported.

Table 3-10 Discrete Options Register (Read Only)

Bit	Field	Definition
0	-	Not used
1	DISC1	Discrete #1 (Set if present; clear if not present)
2	DISC2	Discrete #2 (Set if present; clear if not present)
...	...	...
31	DISC31	Discrete #31 (Set if present; clear if not present)

Differential Options Register (Dbl Wd 0x0E, Bytes 0x38 – 0x3B)

This register provides a bit for each potential differential I/O (up to 31). A bit value of 0 indicates that the differential I/O is not supported.

Table 3-11 Differential Options Register (Read Only)

Bit	Field	Definition
0	-	Not used
1	DIFF1	Differential #1 (Set if present; clear if not present)
2	DIFF2	Differential #2 (Set if present; clear if not present)

Bit	Field	Definition
...	...	...
31	DIFF31	Differential #31 (Set if present; clear if not present)

3.2.2 PIO Options Register (Dbl Wd 0x0F, Bytes 0x3C – 0x3F)

This register provides a bit for each potential PIO I/O (up to 31). A bit value of 0 indicates that the PIO I/O is not supported.

Table 3-12 PIO Options Register (Read Only)

Bit	Field	Definition
0	PIO0	Differential #0 (Set if present; clear if not present)
1	PIO1	Differential #1 (Set if present; clear if not present)
2	PIO2	Differential #2 (Set if present; clear if not present)
...	...	...
31	PIO31	Differential #31 (Set if present; clear if not present)

NOTE

PIOs normally start at #1.

3.2.3 Board Registers (Dbl Wd 0x20 – 0x2F, Bytes 0x80 – 0xBF)

FPGA Revision (Dbl Wd 0x20, Bytes 0x80 – 0x83)

The FPGA Revision is defined below.

Table 3-13 FPGA Revision Register (Read Only)

Bit	Field	Definition
31-0	fpga_rev	FPGA Revision

Interrupt Status (Dbl Wd 0x21, Bytes 0x84 – 0x87)

Each of the individual LPU interrupts is echoed here as well as the ARINC interrupt on ARINC boards so the user can quickly see which device generated an interrupt.

Table 3-14 Interrupt Status Register (Read Only)

Bit	Field	Definition
7-0	1553_int_stat	1553 Interrupt Status Interrupts from the various 1553 devices. When set, an interrupt is pending. When cleared, there is no interrupt. Bit 0 indicates an interrupt from 1553 channel 1; Bit 1 indicates an interrupt from 1553 channel 2, etc.
8	Arinc_int_stat	ARINC Interrupt Status When set, an ARINC interrupt is pending. When cleared, there is no ARINC interrupt.
31-9	0x000000	

User RAM Start Address (Dbl Wd 0x22, Bytes 0x88 – 0x8B)

This byte offset value identifies the offset from the card's base address, where the user's RAM starts.

Table 3-15 User RAM Start Address Register (Read Only)

Bit	Field	Definition
23-0	ram_start	User RAM Start Location Identifies the byte offset from the cards base address where the user RAM starts.
31-24	0x00	

As an example, if a board occupies an 8-MByte address space, it usually has 4 MBytes of RAM which would be in the upper half of the address space. If that were the case, the User RAM Start Address would be 4 MBytes (0x400000).

User RAM Length (Dbl Wd 0x23, Bytes 0x8C – 0x8F)

This byte value identifies the contiguous user RAM available on the card.

Table 3-16 User RAM Length Register (Read Only)

Bit	Field	Definition
23-0	ram_len	User RAM Length Identifies the byte length of user RAM.
31-24	0x00	

As an example, a board with 4 MBytes of user RAM would have a User RAM Length of 0x400000.

LED Control (Dbl Wd 0x24, Bytes 0x90 – 0x93)

This register allows the user to control the BIT (built-in-test) pass and fail LEDs if equipped and individually override each of the onboard 1553 activity LEDs for use as a diagnostic tool.

When the LED Overwrite Enable (ORIDE) bit is set, a channel's LEDs can be controlled as defined by the LED_CH, RED and GRN bits. Refer to the MIL-STD-1553 Hardware Installation and Reference Manual for more information on the "1553 bus activity" LEDs used for your specific board.

For BIT, the API drives the BIT Pass (BITP) and BIT Fail (BITF) LEDs if equipped after a successful or failed pass of BIT. Default for both LEDs is off, and an API Exit should also turn off the LEDs. It is not necessary to set the ORIDE bit to control the BIT LEDs since this is the only way to control them.

Reading this register, as defined in Table 3-17, shows the status of the BIT LEDs and which channel LEDs have been overwritten by the user and their state.

Table 3-17 LED Control Register (Write)

<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>3-0</td><td>led_ch</td><td>LED Channel
The address of the LED being controlled as listed in the table below.

<table><tr><td>LED_CH[3:0]</td><td>Function</td></tr><tr><td>0000</td><td>BIT Led</td></tr><tr><td>0001</td><td>Ch1 Led</td></tr><tr><td>0010</td><td>Ch2 Led</td></tr><tr><td>0011</td><td>Ch3 Led</td></tr><tr><td>0100</td><td>Ch4 Led</td></tr><tr><td>…</td><td>…</td></tr></table></td></tr>
<tr><td>7-4</td><td>Reserved</td><td></td></tr>
<tr><td>8</td><td>grn</td><td>Green Led
Setting this bit turns the green LED on for the channel. Clearing this bit turns the LED off.</td></tr>
<tr><td>9</td><td>red</td><td>RED Led
Setting this bit turns the red LED on for the channel. Clearing this bit turns the LED off.</td></tr>
<tr><td>11-10</td><td>Reserved</td><td></td></tr>
<tr><td>12</td><td>oride</td><td>Over-Ride
Setting this bit allows the host to control the selected channel LEDs. Clearing this bit for a selected channel allows the normal 1553 bus activity sources to control the selected channel LEDs. This bit is not necessary to control the BIT LEDs.</td></tr>
<tr><td>31-13</td><td>Reserved</td><td></td></tr>
</table>

Table 3-18 LED Control Register (Read)

Bit	Field	Definition
0	grn_ch1	Green activity LED for ch1 When set, the green LED will be on.
1	grn_ch2	Green activity LED for ch2 When set, the green LED will be on.
2	grn_ch3	Green activity LED for ch3 When set, the green LED will be on.
3	grn_ch4	Green activity LED for ch4 When set, the green LED will be on.
4	red_ch1	Red activity LED for ch1 When set, the red LED will be on.
5	red_ch2	Red activity LED for ch2 When set, the red LED will be on.
6	red_ch3	Red activity LED for ch3 When set, the red LED will be on.

Bit	Field	Definition
7	red_ch4	Red activity LED for ch4 When set, the red LED will be on.
13-8	Reserved	
14	bitp	BIT Pass When set, the green LED will be on
15	bitf	BIT Fail When set, the red LED will be on.
31-16	Reserved	

Temperature Sensing

Several products contain a temperature sensing IC which can provide the temperature locally, at the sensor IC itself, and externally using remote sensors (diode connected transistors) located near specific board components.

Table 3-19 lists the temperature-sensing IC used per product, as well as the component (with reference designator) near the external-sensing diode.

Table 3-19 Temperature Sensors

Product	IC	Temp 1	Temp 2	Temp 3	Temp 4	Temp 5
LPCIe-1553	MAX6658	Temp sensor (U2)	-	-	-	-
RAR15XMC-XT RAR15XMC-IT	MAX1668	Temp sensor (U8)	FPGA (U4)	RAM (U1)	1553 ch4 board edge (U29)	1553 ch2 mid-board (U32)
RAR15XMC-FIO	MAX1668	Temp sensor (U8)	DC/DC (U34)	FPGA (U25)	RAM (U26)	1553 ch1 (U1)

Temp Sensor Read Command (Dbl Wd 0x25, Bytes 0x94 – 0x97)

The Temp Sensor Read Command Register allows the reading of various registers within the temp sensing IC through the Read Byte format only. Refer to the appropriate temp sensing IC datasheet for more detailed information.

NOTE

After writing the Command Byte, you must wait a minimum of 700 μs before the data is available to read.

Table 3-20 Temp Sensor Read Command Register (Write)

Bit	Field	Definition
7-0	cmd	Command Byte Writing a command to this register provides various data from within the temperature sensing IC.

cmd	Function
0x00	Read Temp 1
0x01	Read Temp 2
0x02	Read Temp 3

Bit	Field	Definition
		0x03 Read Temp 4 0x04 Read Temp 5 Refer to the MAX6658 / MAX1668 datasheets for further command byte functions.
31-8	Reserved	

Table 3-21 Temp Sensor Read Command Register (Read)

Bit	Field	Definition
7-0	rd	Read Data Reads data as addressed by the Command Byte above.
8	otn	For boards using the MAX6658: This bit is connected to the OVERT1~ output. For boards using the MAX1668: This bit is connected to the ALERT output.
31-9	Reserved	

As an example, to read the MAX6658 Manufacture ID, write a 0xFE, the Read Manufacturer ID address. After 700 µs, read this register to get the devices Read Manufacturer ID, 0x14D, in the lower 8 bits with the OTN bit set indicating the temperature alarm has not been set. To read the board temperature, write a 0x0, the address to read the MAX6658 internal temperature. After 700 µs, you would read this register where the lower 8 bits is the board two's complement temperature in degrees Celsius (C°). A returned value of 0x19 would convert to 25 C°, whereas a value of 0xE7 corresponds to -25 C° (0xFF – 0xE7 + 1).

Temp Sensor Write Command (Dbl Wd 0x26, Bytes 0x98 – 0x9B)

Several products contain a temperature sensing IC with one or more temp sensing channels, providing the temperature near several board components. Additionally, an over-temperature alarm, with and adjustable set point is available.

This register allows the writing of commands to the device via the Write Byte format only. Refer to the device datasheet for more information.

Table 3-22 Temp Sensor Write Command Register (Write)

Bit	Field	Definition
7-0	cmd[7:0]	Command Byte Selects the register you are writing to within the MAX6658.
15-8	wdb[7:0]	Write Data Byte Used to set thresholds, configuration masks and sampling rate.
31-16	Reserved	

System Reset Control (Dbl Wd 0x27, Bytes 0x9C – 0x9F)

This register allows the user to control whether the avionics logic on the board is reset during a computer warm boot (reboot). When enabled, the logic and embedded FPGA processor will be reset. This will not reload the FPGA and will not affect data in memory other than what the embedded FPGA initializes.

Table 3-23 System Reset Control Register (Read/Write)

Bit	Field	Definition
0	esr	Enable System Reset Setting this bit will enable the System Reset (e.g. PCI / PCIe Reset) signal to clear all avionics logic on the board. Clearing this bit, which is the default, does not enable the resetting of the avionics logic. This bit is readable.
31-1	Reserved	

3.2.4 I/O Registers (Dbl Wd 0x30 – 0x4F, Bytes 0xC0 – 0x13F)

NOTE

The I/O Registers described below may or may not apply to your product and if they do, channel counts may vary. Reference the "MIL-STD-1553 Hardware Installation and Reference Manual" to determine the I/O capability of your product.

Discrete Out (Dbl Wd 0x30, Bytes 0xC0 – 0xC3)

General purpose Avionics Discrete outputs are implemented as low-side switches. They are controlled one at a time by writing channel and drive data as described in the "Write" table below (Table 3-24). Reading this register returns the state of how each of the discrete outputs is being driven.

For a discrete to be an input, the corresponding discrete output must be turned off, which is the default condition on power for all switches. Note that some boards use discretes as inputs for an External RT Address, so care must be taken to make sure those discretes are turned off.

Discretes can be used as triggers on boards without dedicated triggers. The trigger function is ORed with the discrete output control below which allows for manual testing of the trigger.

Table 3-24 Discrete Out Register (Write)

<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>4-0</td><td>disc_ch [4:0]</td><td>Discrete Channel
Selects the available discrete as shown in the embedded table below.
<table>
<tr><th>DISC_CH[4:0]</th><th>Discrete Channel</th></tr>
<tr><td>00000</td><td>Not used</td></tr>
<tr><td>00001</td><td>Discrete1</td></tr>
<tr><td>00010</td><td>Discrete2</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>01100</td><td>Discrete12</td></tr>
<tr><td>…</td><td>…</td></tr>
</table></td></tr>
<tr><td>7-5</td><td>Reserved</td><td></td></tr>
</table>

Bit	Field	Definition
8	drv_dat	Drive Data Setting this bit causes the low side switch to be turned on, thus pulling the discrete channel to ground. Clear this bit to turn off the low side switch which causes the selected discrete to be pulled up to 3.3V via a weak pullup.
31-9	Reserved	

Table 3-25 Discrete Out Register (Read)

Bit	Field	Definition
0	N/A	Not used
31-1	disc_drive_data [31:1]	Discrete Drive Data Drive data for up to 31 channels, where bit 1 is the drive data for discrete 1, bit 2 is the drive data for discrete 2, etc. If a bit is set, it indicates that the low side switch is being driven, and its output should be low. If a bit is cleared, it indicates that the low side switch is not being driven, and its output should be pulled high.

Discrete In (Dbl Wd 0x31, Bytes 0xC4 – 0xC7)

This register provides the status of the Discrete I/O pins. If the voltage present at a discrete I/O pin is +1.4 VDC or less, the associated bit reads a "0", while voltages greater than +2.0 VDC return a "1".

Table 3-26 Discrete In Register (Read Only)

Bit	Field	Definition
0	N/A	Not used
31-1	disc_rcv_data [31:1]	Discrete Receive Data Receive data for up to 31 channels, where bit 1 monitors discrete I/O 1, bit 2 monitors discrete I/O 2, etc. If a bit is set, then the discrete line is high. If a bit is cleared, then the discrete line is low.

RS485 Transmit & Control (Dbl Wd 0x32, Bytes 0XC8 – 0xCB)

This register controls all RS485 outputs, one at a time. To set up the RS485 I/O, you need to select the channel (485_CH) and set the appropriate data (DAT), transmit enable (TXEN) and termination (TERM) bits as required.

When TXEN is set, the device transmits the value set by the DAT bit. To set up a 485 channel as a receiver, clear the TXEN.

Some boards offer a switchable 120-ohm resistor as part of the 485 transceiver. If your board has this feature, setting the TERM bit enables the termination.

The power default for RS485 devices is that they are set up as receivers with the termination (if available) disabled.

RS485 outputs can be used as triggers on boards without dedicated triggers. The trigger function is ORed with the RS485 output control below which allows for

manual testing of the trigger. When an RS485 channel is used as a trigger output, the associated TXEN must be set.

Table 3-27 RS485 Transmit and Control Register (Write)

<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>3-0</td><td>485_ch [3:0]</td><td>485 Channel
Selects a 485 differential channel as shown in the table below.
<table>
<tr><td>485_CH[3:0]</td><td>Differential Channel</td></tr>
<tr><td>0x0</td><td>Not used</td></tr>
<tr><td>0x1</td><td>Diff1</td></tr>
<tr><td>0x2</td><td>Diff2</td></tr>
<tr><td>0x3</td><td>Diff3</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>0x8</td><td>Diff8</td></tr>
<tr><td>…</td><td>…</td></tr>
</table></td></tr>
<tr><td>7-4</td><td>Reserved</td><td></td></tr>
<tr><td>8</td><td>dat</td><td>Data
Set this bit for 485 + pin = “1” and 485 - pin = “0”.
Clear the bit for 485+ pin = “0” and 485- pin = “1”.</td></tr>
<tr><td>9</td><td>txen</td><td>Transmit Enable
Set the bit for the 485 device to transmit, or clear the bit for the device to receive.</td></tr>
<tr><td>10</td><td>term</td><td>Termination
Setting this bit enables a 120-ohm termination within the 485 transceiver. Clear this bit for no termination.
This feature is board specific.</td></tr>
<tr><td>31-11</td><td>Reserved</td><td></td></tr>
</table>

The reading of this register provides transmit enable and termination status. Only those channels supported by a board provide valid data.

Table 3-28 RS485 Transmit and Control Register (Read)

Bit	Field	Definition
0	N/A	Not used
15-1	485_txen[15:1]	RS485 Transmit Enable Status for up to 15 channels. Set indicates the corresponding 485 device is transmitting. When clear, the corresponding 485 device is configured to receive.
16	N/A	Not used
31-17	485_term[15:1]	RS485 Termination Status for up to 15 channels. Set indicates the corresponding 120-ohm termination within the 485 transceiver is enabled. If cleared, the corresponding termination is not enabled. This feature is board specific.

RS485 Data (Dbl Wd 0x33, Bytes 0xCC – 0xCF)

This read-only register provides both the data that the 485 transceiver is receiving and the drive data that is being provided to the transmitter.

Only those channels supported by a board provide valid data.

Table 3-29 RS485 Transmit and Receive Data (Read Only)

Bit	Field	Definition
0	N/A	Not used
15-1	485_rcv_data [15:1]	RS485 Receive Data RS485 + receive data for up to 15 channels. The corresponding bit indicates the input on the associated RS485 + pin.
16	N/A	Not used
31-17	485_xmit_data [15:1]	RS485 Transmit Data RS485 + transmit data for up to 15 channels. The corresponding bit indicates the data that is being transmitted to the associated RS485 + pin, assuming the respective RS485 Transmit Enable is set.

External RT Address (Dbl Wd 0x34, Bytes 0xD0 – 0xD3)

This register provides the External RT Address presented at the external card edge connector or on some boards, hardwired on the card. It is used as a test aid for hardware verification and is not supported in the API. For boards that use discretes for RT Addressing, those values echo here as well as in Discrete In (DW 0x31) register. If a dedicated external pin or onboard selection is used to enable the external RT Address, it can also be read here.

NOTE

External RT addressing can vary between products, so reference the board's documentation for external RT addressing options and availability.

The returned data is only valid for External RT Addresses installed on the card. If External RT Addressing is not available, this register should return 0x0.

Some boards can have Flash-based RT Addressing and/or Flash-based RT Offsets, where a channel has an RT address offset from the external RT address (provided here). To read the actual RT address presented to a specific 1553 channel, you need to read the Hardwired RT Address as defined in the "LPU Reference Manual".

Table 3-30 External RT Address Register (Read Only)

Bit	Field	Definition
5-0	ext_rt_addr _ch1	External RT Address for channel 1 The RT address is defined by ext_rt_addr[4:0] where bit 0 is the LSB of the address. The address parity bit is ext_rt_addr[5].
6	hwrt_en _ch1	Hardwired External RT Enable pin (if available) This bit is low-true, so "0" indicates that External RT Addressing for channel 1 is being used.
7	Reserved	

Bit	Field	Definition
13-8	ext_rt_addr _ch2	See ext_rt_addr _ch1.
14	hwrt_en _ch2	See hwrt_en _ch1.
15	Reserved	
21-16	ext_rt_addr _ch3	See ext_rt_addr _ch1.
22	hwrt_en _ch3	See hwrt_en _ch1.
23	Reserved	
29-24	ext_rt_addr _ch4	See ext_rt_addr _ch1.
30	hwrt_en _ch4	See hwrt_en _ch1.
31	Reserved	

DAC Control Register (Dbl Wd 0x36, Bytes 0xD8 – 0xDB)

This register controls the 1553 D/A Converters (DACs) for varying the transceiver output voltage (if the board supports variable voltage), as well as the IRIG DAC, for setting the detection level (if the board supports IRIG).

Table 3-31 DAC Control Register (Write Only)

Bit	Field	Definition
7-0	data[7:0]	Data Bit 7 is the MSB.
11-8	dac[3:0]	DAC Address DACs are identified in the embedded table below.
12	a_b	A or B DAC Side Each DAC device is comprised of two DACs. Set per the table above.
13	vsel	high = 95 mV/step, low = 20 mV/step For +3.3 V variable-voltage 1553 transceivers only.
31-14	Reserved	

A_B	DAC[3:0]	Function Implemented
0	0000	CH 1 1553 Variable Volt
1	0000	CH 2 1553 Variable Volt
0	0001	CH 3 1553 Variable Volt
1	0001	CH 4 1553 Variable Volt
0	1000	IRIG Threshold
1	1000	Discrete Threshold (some boards)

1553

The 1553 DAC(s) allows a 1553 channel to vary its output from 0 to 0xFF full scale (0 to 255 decimal). The default sets each output to full scale. Some boards (RAR15XMC-FIO) have a voltage step selection (vsel) bit which allows the DAC to operate at finer

resolutions over a constrained range of bus voltages[5] for enhanced ability to test bus low-level characteristics.

IRIG

The IRIG DAC sets the threshold level for detecting either AM or DC level shifted IRIG data. The threshold is set according to the formula below where n is the decimal equivalent of data[7:0}:

$V_{threshold} = 3.3V \times n/255$

The default value written to this register is 0x9B (155 decimal), which sets the threshold voltage at 2 V. This register is valid for all boards, except for the PCCARD-1553. The PCCard-1553 receives only DC-Level Shifted IRIG, and the IRIG calibration routine is unnecessary for this card.

NOTE

When programming a DAC, wait a minimum of 2 μs from the time the DAC is written to the time the IRIG or 1553 device is used to allow for DAC programming and settling time.

PIO Control Register (Dbl Wd 0x37, Bytes 0xDC – 0xDF)

This register controls the bidirectional TTL-level Programmable I/O (PIO) signals. They are controlled one at a time by writing channel, level and direction as described in the "Write" table below. Reading this register returns the state of each individual PIO input pin.

Table 3-32 PIO Control Register (Write)

<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>4-0</td><td>pio_ch [4:0]</td><td>PIO Channel
Selects the available PIO as shown in the embedded table below.
<table>
<tr><td>PIO_CH[4:0]</td><td>PIO Channel</td></tr>
<tr><td>00000</td><td>PIO0</td></tr>
<tr><td>00001</td><td>PIO1</td></tr>
<tr><td>00010</td><td>PIO2</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>11111</td><td>PIO31</td></tr>
<tr><td>…</td><td>…</td></tr>
</table></td></tr>
<tr><td>7-5</td><td>Reserved</td><td></td></tr>
<tr><td>9-8</td><td>set_level[1:0]</td><td>Set the output levels as follows:
<table>
<tr><td>Set_level [1:0]</td><td>Output Level</td></tr>
<tr><td>00</td><td>No change in output level</td></tr>
<tr><td>01</td><td>Sets the output level to a zero</td></tr>
<tr><td>10</td><td>Sets the output level to a one</td></tr>
<tr><td>11</td><td>Not allowed</td></tr>
</table></td></tr>
</table>

[5] Typically, 0-5 V line-to-line, transformer coupled

<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>11-10</td><td>set_dir[1:0]</td><td>Set the output levels as follows:
<table>
<tr><th>Set_dir [1:0]</th><th>Output Level</th></tr>
<tr><td>00</td><td>No change in direction</td></tr>
<tr><td>01</td><td>Disables or tri-states output driver (pin is configured as an input)</td></tr>
<tr><td>10</td><td>Enables output driver (pin is configured as an output)</td></tr>
<tr><td>11</td><td>Not allowed</td></tr>
</table></td></tr>
<tr><td>31-12</td><td>Reserved</td><td></td></tr>
</table>

Table 3-33 PIO Control Register (Read)

Bit	Field	Definition
31-0	PIO_data [31:0]	PIO input data Data for up to 32 PIO channels where bit 0 monitors PIO 0, bit 1 monitors PIO 1, etc. This value represents the state of the PIO pin, regardless of whether it's configured as an input or an output. If a bit is set, then the PIO signal is high. If a bit is cleared, then the PIO signal is low.

3.2.5 Timing Registers (Dbl Wd 0x50 – 5F, Bytes 0x140 – 0x17F)

IRIG Control Register (Dbl Wd 0x50, Bytes 0x140 – 0x143)

For boards that support IRIG, this register allows the user to calibrate the input level detection in conjunction with the IRIG DAC. Additionally, you can see if the board has locked to the incoming IRIG signal, loop back IRIG internally for test and control the IRIG output if available.

NOTE

All bits can be read but only bit1 and bit2 are writable.

Table 3-34 Timing Register (Read/Write)

Bit	Field	Definition
0	cal	Calibrate (Read Only) Set when the conditioned IRIG input is receiving data based on the threshold set with the IRIG DAC. This bit is cleared when the read is completed. This value is always set for the PCCARD-1553, as it receives only DC level shifted IRIG. This bit is used in conjunction with the IRIG DAC to calibrate the internal threshold of the Amplitude Modulation signal-conditioning circuitry. By scanning the threshold range for upper and lower bounds of valid signal, the threshold may be set for approximately 80% of the valid signal range for maximum reliability.
1	out	IRIG Output Enable (Read/Write) This bit is the output enable for the IRIG output. When set, the internal IRIG

Bit	Field	Definition
		encoder outputs valid IRIG data based on the TOY (Time of Year) data. When cleared, the output is driven low. For PCCARD-1553 boards, setting this bit routes IRIG signals through the card's External In and External Out signal pins, respectively. Care must be exercised when using IRIG or Trig I/O, as the pins are dual-purpose. Power-up default is to Trig I/O. This bit is known as irig_status[1] in the firmware.
2	int	Internal IRIG Source (Read/Write) This bit determines the IRIG source in use. When set, the IRIG source is the onboard IRIG generator and the External IRIG Input is ignored. When cleared, the External IRIG Input is routed to the onboard IRIG Decoder. This bit is known as irig_status[2] in the firmware.
3	val	Valid IRIG Timecode (Read Only) Set if IRIG time code input is valid; otherwise, clear.[6]
31-4	Reserved	

IRIG TOY (Dbl Wd 0x51, Bytes 0x104 – 0x107)

The IRIG Time of Year (TOY) is presented as 30 bits of information. All fields are set to 0x0 on power or software reset.

Table 3-35 IRIG TOY Register (Write Only)

Bit	Field	Definition
3-0	sec[3:0]	Units of seconds
6-4	secx10[2:0]	Tens of seconds
10-7	min[3:0]	Units of minutes
13-11	Minx10[2:0]	Tens of minutes
17-14	hr[3:0]	Units of hours
19-18	hrx10[1:0]	Tens of hours
23-20	day	Units of days
27-24	dayx10	Tens of days
29-28	dayx100	Hundreds of days
31-30	Reserved	

Reset All TTC's (Dbl Wd 0x52, Bytes 0x108 – 0x10B)

This register is used to synchronize all the 1553 Time Tag Counters by resetting all of them at the same time to 0x0.

Table 3-36 Time Tag Counter Reset Register (Write Only)

Bit	Field	Definition
0	rst all ttcs	Reset all Time Tag Counters Setting this bit causes all Time Tag Counters to be reset to 0x0.

[6] It may take over 1 second for the IRIG decoder to update the Valid flag after the connection and calibration of a valid IRIG signal.

Bit	Field	Definition
31-1	Not used	

3.2.6 FPGA ADC (Dbl Wd 0x100 – 0x106, Bytes 0x400 – 0x41B)

The R15-MPCIE's Xilinx Atrix 7 FPGA contains dual 12- bit ADCs which are available for use with both external analog inputs and on-chip sensors. The external input allows the monitoring of the board's 3.3 V supply. The internal inputs monitor the die temperature, Vccint, Vccaux and Vccbram supplies. The ADC is configured (in the firmware) to automatically and continuously sample each of the above-mentioned channels and averages each channel 16 times before being made available to the registers defined below. Sampling each channel 16 times takes close to 180 µs. There is no collision avoidance on the registers, so it is possible that the ADC could write a value while the host does a read. It is up to the host to ferret out "bad" reads.

FPGA Die Temp (Dbl Wd 0x100, Bytes 0x400 – 0x403)

The FPGA Die temperature is determined from the function:

Temperature (°C) = (ADC Code × 503.975/4096) - 273.15

Table 3-37 FPGA Die Temperature Register (Read Only)

Bit	Field	Definition
3-0	Not used	
15-4	adc_code	FPGA ADC conversion output
31-16	Not used	

FPGA Vccint Supply Voltage (Dbl Wd 0x101, Bytes 0x404 – 0x407)

The Vccint supply should nominally be 1.0 V and is the same supply as Vccbram. The supply voltage is determined from the function below:

Voltage = ADC Code x 3V/4096

Table 3-38 FPGA Vccint Supply Voltage Register (Read Only)

Bit	Field	Definition
3-0	Not used	
15-4	adc_code	FPGA ADC conversion output
31-16	Not used	

FPGA Vccaux Supply Voltage (Dbl Wd 0x102, Bytes 0x408 – 0x40B)

The Vccaux supply should nominally be 1.8 V. The supply voltage is determined from the function below:

Voltage = ADC Code x 3V/4096

Table 3-39 FPGA Vccaux Supply Voltage Register (Read Only)

Bit	Field	Definition
3-0	Not used	
15-4	adc_code	FPGA ADC conversion output
31-16	Not used	

Board Vcc Supply Voltage (Dbl Wd 0x103, Bytes 0x40C – 0x40F)

The Vcc supply to the board is nominally 3.3V but can swing from 3.0 – 3.6V. The supply voltage is determined from the function:

Board Vcc = ADC Code x 0.001

Table 3-40 FPGA Vcc Supply Voltage Register (Read Only)

Bit	Field	Definition
3-0	Not used	
15-4	adc_code	FPGA ADC conversion output
31-16	Not used	

FPGA Vccbram Supply Voltage (Dbl Wd 0x106, Bytes 0x418 – 0x41B)

The Vccbram supply should nominally be 1.0 V and is the same supply as Vccint. The supply voltage is determined from the function below:

Voltage = ADC Code x 3V/4096

Table 3-41 FPGA Vccbram Supply Voltage Register (Read Only)

Bit	Field	Definition
3-0	Not used	
15-4	adc_code	FPGA ADC conversion output
31-16	Not used	

4 • Channel-Specific Registers

This chapter describes the 1553 channel-specific registers. A memory map of the 1553 channel-specific registers is shown in Table 4-1, followed by the individual register descriptions. The File Registers for each 1553 channel are described in the MIL-STD-1553 Enhanced Universal Core Architecture (UCA32) Local Processing Unit (LPU) Reference Manual. The Enable column is for internal reference only.

Table 4-1 1553 Channel-Specific Register Memory Map

Global Registers	Read /Write	Double Word Offset	Byte Offset	Enable (Decimal)
Channel-Specific Registers (File, Time Tag & Trigger Registers)				
CH 1				
File Registers	R/W	0xC000 - 0xC0FF	0x30000 - 0x303FF	
Time Tag (TT) Control	W	0xC400	0x31000	50176
TT Load Lower	W	0xC401	0x31004	50177
TT Load Upper	W	0xC402	0x31008	50178
TT Increment	W	0xC403	0x3100C	50179
TT Readback Load	W	0xC404	0x31010	50180
TT Readback Lower	R	0xC405	0x31014	50181
TT Readback Upper	R	0xC406	0x31018	50182
Trigger Input Control	R/W	0xC800	0x32000	51200
Trigger Output Control	R/W	0xC801	0x32004	51201
CH 2				
File Registers	R/W	0xD000 - 0xD0FF	0x34000 - 0x343FF	
Time Tag (TT) Control	W	0xD400	0x35000	54272
TT Load Lower	W	0xD401	0x35004	54273
TT Load Upper	W	0xD402	0x35008	54274
TT Increment	W	0xD403	0x3500C	54275
TT Readback Load	W	0xD404	0x35010	54276
TT Readback Lower	R	0xD405	0x35014	54277
TT Readback Upper	R	0xD406	0x35018	54278
Trigger Input Control	R/W	0xD800	0x36000	55296
Trigger Output Control	R/W	0xD801	0x36004	55297
CH 3				
File Registers	R/W	0xE000 - 0xE0FF	0x38000 - 0x383FF	
Time Tag (TT) Control	W	0xE400	0x39000	58368
TT Load Lower	W	0xE401	0x39004	58369

Global Registers	Read /Write	Double Word Offset	Byte Offset	Enable (Decimal)
Channel-Specific Registers (File, Time Tag & Trigger Registers)				
TT Load Upper	W	0xE402	0x39008	58370
TT Increment	W	0xE403	0x3900C	58371
TT Readback Load	W	0xE404	0x39010	58372
TT Readback Lower	R	0xE405	0x39014	58373
TT Readback Upper	R	0xE406	0x39018	58374
Trigger Input Control	R/W	0xE800	0x3A000	59392
Trigger Output Control	R/W	0xE801	0x3A004	59393
CH 4				
File Registers	R/W	0xF000 - 0xF0FF	0x3C000 - 0x3C3FF	
Time Tag (TT) Control	W	0xF400	0x3D000	62464
TT Load Lower	W	0xF401	0x3D004	62465
TT Load Upper	W	0xF402	0x3D008	62466
TT Increment	W	0xF403	0x3D00C	62467
TT Readback Load	W	0xF404	0x3D010	62468
TT Readback Lower	R	0xF405	0x3D014	62469
TT Readback Upper	R	0xF406	0x3D018	62470
Trigger Input Control	R/W	0xF800	0x3E000	63488
Trigger Output Control	R/W	0xF801	0x3E004	63489

4.1 Channel-Specific Global Registers

4.1.1 Time Tag Registers

Each 1553 channel has its own dedicated 64-bit Time Tag Counter (TTC) used to timestamp the channel's data in 1553 RT and Monitor modes. The TTC may also be used as a high-resolution general-purpose timer for the host. The resolution of the 64-bit time is 1 ns; however, the clock rate at which the timer increments is based on the operating frequency of the timer logic. In most cases, the timer operates at 40 MHz which means the timer updates every 25 ns.

The TTC is a free-running timer that is initialized during the power up sequence. There are several capabilities to load, synchronize and to read the TTC.

The TTC Control (TTCC) register controls loading of the TTC. Three modes of operation are supported: one software mode and two hardware modes. Boards that support IRIG can also load the TTC with IRIG time.

The TTC Load (TTCL) register is a write-only 64-bit register used for loading a value into the TTC. The software first loads this register with the desired value. Then,

using the TTCC register, commands the hardware to load the value of the TTCL into the TTC.

The TTC Increment register (TTCI) is a 32-bit register that is used to increment the TTC in auto-increment mode. The software first loads this register with the desired value. Then, using the TTCC register, commands the hardware to increment the TTC by this value whenever an external input pulse occurs. The LSB of the TTCI is aligned with the LSB of the TTCL register.

The TTC may be directly read by the host through the Time Tag Readback (TTR) Lower & Upper registers which allows it to be used as a high-resolution general-purpose timer. Writing any value to the Time Tag Readback Load (TTRL) register latches the current time. This allows the user to read the latched time via the TTR registers.

There is a Global "Reset All Time Tag Registers" (DW 0x52) function which synchronizes all the Time Tag Counters by resetting each of them to 0x0.

The various time tag registers and address locations listed below are for channel 1. Reference the memory map in Table 4-1 for address locations of additional channels that your board may support.

Ch1 Time Tag Counter Control Register (Dbl Wd 0xC400, Bytes 0x31000 – 0x31003)

The TTC Control (TTCC) Register controls loading of the TTC. Three modes of operation are supported: one software mode and two hardware modes. The hardware modes allow either loading of the TTC through software intervention or auto-incrementing the TTC without software intervention. Boards that support IRIG can also load the TTC with IRIG time. The TTC Control Register cannot be read back by the host.

The RXMC2 supports an external clock and reset input for control of the TTC. These inputs may be enabled by setting their respective bits in this register. The external clock edge (CKE) bit may be used to specify whether the rising edge or falling edge of the external clock is used to increment the counter when enabled.

Table 4-2 Channel 1 TTC Control Register (Write Only)

Bit	Field	Definition
0	hwl	Hardware Load TTC Setting this bit forces the TTC to be loaded with the contents of the time tag counter load register (TTCL) with each low to high pulse on the TTL input pin. This allows for external synchronization of the time tag. When the TTC is loaded, an interrupt to the host is generated. This allows the host software to load the value in the TTCL for the next external sync pulse. The TTCL register must be loaded prior to setting this bit. It is recommended to use the auto-increment mode rather than hardware load tag counter mode.
1	swl	Software Load TTC Setting this bit forces the TTC to be loaded with the contents of the time tag

Bit	Field	Definition
		counter load register (TTCL). The TTCL register must be loaded prior to setting this bit. This mode may be used with an appropriate software routine to increment the TTC upon each interrupt from an external synchronizing source.
2	irig	Load TTC with IRIG Decoder (option) Setting this bit forces the TTC to be loaded with the contents of the IRIG decoder with the 1pps input signal.
3	auto	Automatically Increment TTC Setting this bit forces the TTC to be incremented by the contents of the time tag counter increment register (TTCI) with each low to high pulse on the TTL input pin. This allows for external synchronization of the time tag without software intervention. The TTCI register must be loaded prior to setting this bit. If interrupts are desired when the load occurs, set the hardware load tag counter bit to generate the interrupts.
4	Reserved	
5	ece	External Clock Enable (RXMC2)
6	cke	External Clock Edge (RXMC2) Clear to use rising edge. Set to use falling edge.
7	ere	External Reset Enable (RXMC2)
15-8	Reserved	
25-16	einc	External Increment Count (RXMC2) When an external clock is enabled (ece = 1), this value tells the TTC how much to increment every time it gets an external clock input. The frequency at which the TTC runs must also be considered in setting this value. If the TTC runs at 40 MHz, the counter increments every 25 ns. Since the resolution of the time tag register is 1ns, every clock adds 25 ns to the time tag count. For an external 1 MHz clock to count in 1-μs increments, every clock pulse must add 1000 to the time tag count.
31-26	Reserved	

Ch1 Time Tag Counter Load Lower Register (Dbl Wd 0xC401-0xC402, Bytes 0x31004 – 0x3100B)

The TTC Load register (TTCL) is a write-only 64-bit register used for loading a value into the TTC. The resolution of this register is 1 ns. The software first loads this register with the desired value, then, using the TTC register, commands the hardware to load the value of the TTCL into the TTC. The hardware insures that this load is an atomic operation to insure the correct initialization of the TTC.

The hardware supports three modes of loading the TTCL into the TTC: a software mode, a hardware mode and an automatic mode. These modes are described in the TTCC register description.

Table 4-3 Channel 1 Time Tag Counter Load Lower Register (Write Only)

Bit	Field	Definition
Dbl Wd 0xC401, Bytes 0x31004-0x31007		
31-0	ttcl[31:0]	TTC Load Register This register spans 2 double data words. These registers have 1 ns resolution and are loaded into the TTC as instructed by the TTCC register.
Dbl Wd 0xC402, Bytes 0x31008-0x3100B		
31-0	ttcl[63:32]	TTC Load Register This register spans 2 double data words. These registers have 1 ns resolution and are loaded into the TTC as instructed by the TTCC register.

Ch1 Time Tag Counter Increment Register (Dbl Wd 0xC403, Bytes 0x3100C – 0x3100F)

The time tag counter increment register (TTCI) is a 32-bit register that is used to increment the 64-bit time tag counter (TTC) in auto-increment mode. The resolution of this register is 1 ns. The software first loads this register with the desired value, then, using the TTCC register, commands the hardware to increment the TTC by this value whenever an external input pulse occurs. The LSB of the TTCI is aligned with the LSB of the TTCL register.

Table 4-4 Channel 1 TTC Increment Register (Write Only)

Bit	Field	Definition
31-0	ttci[31:0]	TTC Increment Register This register has 1 ns resolution and is used when an external input pulse is used and controlled by the TTCC register.

Ch1 Time Tag Readback Load Register (Dbl Wd 0xC404, Bytes 0x31010 – 0x31013)

The TTC may be directly read by the host through the Time Tag Readback (TTR) registers which allows it to be used as a high-resolution general-purpose timer. Writing any value to this Time Tag Readback Load (TTRL) register latches the current time which can then be read via the TTR registers.

Table 4-5 Channel 1 TT Readback Load Register (Write Only)

Bit	Field	Definition
31-0	ttrl[31:0]	TTC Readback Load Register Write any value to this register to load the current TTC value.

Ch1 Time Tag Readback Lower & Upper Registers (Dbl Wd 0xC405-0xC406, Bytes 0x31014 – 0x3101B)

After writing to the Time Tag Readback Load register, the 64 bit TTC data is read with these two registers. The resolution of this register is 1 ns.

Table 4-6 Channel 1 TT Readback Load Register (Read Only)

Bit	Field	Definition
Dbl Wd 0xC405, Bytes 0x31014-0x31017		
31-0	ttc[31:0]	Time Tag Counter Register This register spans 2 double data words and provides the time tag data in 1 ns resolution.
Dbl Wd 0xC406, Bytes 0x31018-0x3101B		
31-0	ttc[63:32]	Time Tag Counter Register This register spans 2 double data words and provides the time tag data in 1 ns resolution.

4.1.2 Trigger Registers

Each 1553 channel can have a trigger input and a trigger output. Input triggers can be for starting the BC, RT or BM functions as well as loading the TTC. Output triggers can provide a BM trigger or RT synchronization-mode code output. The details of the trigger input and output functions can be found in the LPU Reference Manual.

The trigger registers defined below are required for boards that do not have dedicated I/O triggers and are used to define the input trigger source and output trigger target for each 1553 channel. Boards that have dedicated I/O for triggers do not use these registers. The software can determine if there is a dedicated trigger input or output on the board by reading bit 10 of the trigger input control or trigger output control register, respectively.

NOTE

When using a Discrete or RS485 channel as a trigger, that function is ORed with the respective output control which allows for manual testing of the trigger. When an RS485 channel is used as a trigger output, the associated TXEN must be enabled.

The registers listed below are for channel 1. Reference the memory map in Table 4-1 for address locations for additional channels that your board may support.

Trigger Input & Output Control Registers

Both the Trigger Input and Trigger Output Control registers use the same Read/Write Field format listed below.

CH1 Trigger Input Control (Dbl Wd 0xC800, Bytes 0x32000 – 0x32003)

This register selects the trigger input source. Dedicated input triggers (if available) are always assigned to their defined channel. Multiple 1553 channels can share the same non-dedicated (Discretes/Differential/PIO) trigger input source.

NOTE

The source device selected must be set up as an input using the Discrete Out or RS485 Transmit & Control registers.

CH1 Trigger Output Control (Dbl Wd 0xC801, Bytes 0x32004 – 0x32007)

This register selects where to direct the 1553 CH1 trigger output. Multiple 1553 channels can share the same trigger output destination.

NOTE

When configuring a trigger output, the same device and channel must be set up as an input using the Discrete Out or RS485 Transmit & Control registers. Additionally, when an RS485 channel is used as a trigger output, the associated TXEN must be enabled.

Table 4-7 Channel 1 Trigger Input and Output Control Register (Read/Write)

<table>
<tr><th>Bit</th><th>Field</th><th>Definition</th></tr>
<tr><td>4-0</td><td>channel[4:0]</td><td>Trigger Channel
This value is set to indicate the channel of the discrete, differential, or other digital input or output. Reference your board documentation for channel availability. Currently only 18 discrete channels, 3 differential channels, and 8 PIO channels are supported. These bits are ignored when the Trigger Type field selects dedicated input triggers.
<table>
<tr><th>Ch[4:0]</th><th>Source/Destination</th></tr>
<tr><td>0x0</td><td>Not used</td></tr>
<tr><td>0x1</td><td>Ch 1</td></tr>
<tr><td>0x2</td><td>Ch 2</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>0x1F</td><td>Ch 31</td></tr>
</table>
</td></tr>
<tr><td>7-5</td><td>Reserved</td><td></td></tr>
<tr><td>9-8</td><td>type[1:0]</td><td>Trigger Type
This value determines the type of I/O used for the trigger input or output as shown in the embedded table below.
<table>
<tr><th>Type[1:0]</th><th>Source/Destination</th></tr>
<tr><td>0x0</td><td>Dedicated Trigger (default)</td></tr>
<tr><td>0x1</td><td>Discrete (if available)</td></tr>
<tr><td>0x2</td><td>Differential (if available)</td></tr>
<tr><td>0x3</td><td>PIO (if available)</td></tr>
</table>
</td></tr>
<tr><td>10</td><td>dedicated
(read only)</td><td>Dedicated trigger available
0=no dedicated trigger; 1=dedicated trigger available</td></tr>
<tr><td>31-11</td><td>Reserved</td><td></td></tr>
</table>

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