# MIL-STD-1553 Firmware Revisions

**Products covered include:**

- AMC-1553
- cPCI-1553
- IP-1553
- IP-D1553
- PCCARD-1553
- PCCARD-D1553 / RPCC-D1553
- Q104-1553
- Q104-1553P
- QCP-1553
- PCI-1553
- PMC-1553
- QPCI-1553
- QPCX-1553
- QPMC-1553
- QPM-1553
- QVME-1553
- QVXI-1553
- R15-AMC
- R15-EC
- R15-LPCIE
- R15-MPCIE
- R15-USB
- R15-USB-MON
- RAR15-XMC-IT (RAR15-XMC-XT)
- RAR15XF (RAR15-XMC-FIO)
- RPCIE-1553
- RQVME2-1553
- RXMC-1553
- RXMC2-1553
- VME-1553
- VXI-1553

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**Abaco Systems MIL-STD-1553 Firmware Revisions**

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## Additional Resources

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# Overview of Revision Numbering

This document identifies the firmware versions for Abaco Systems MIL-STD-1553 products. The revision numbering scheme changed with Version 6 (V6).

(1) Pre-V6 firmware

Versions 3, 4 and 5 firmware use a single revision number for the firmware build, of the format n.xxbyy, where "n" is the single digit major revision, "xx" is the two digit integer sub-revision, and "yy" is the optional build number. Some examples are 3.70, 4.40b29, and 5.18b2. The firmware revision is identical to the MIL-STD-1553 Local Processing Unit (LPU) revision, so the evolution of the firmware can be traced using the LPU Revision History section.

(2) V6 firmware

There are two distinct revision values associated with V6 firmware:

- The FPGA revision number is an integer that increments with each build of firmware. The revision number represents a distinct firmware build for the FPGA used on the product. FPGA revision numbers are assigned independently for each product. FPGA revision numbers are also used for FPGA development. Multiple FPGA firmware revisions may use the same revision of the LPU.
- The LPU revision number follows the format of 6.xxByy, where "6.xx" is the major MIL-STD-1553 Local Processing Unit (LPU) revision number and "yy" is the sub-revision or build number. The LPU revision identifies the IP source code used for the LPU in the firmware build. The evolution of the MIL-STD-1553 firmware can be traced using the LPU Revision History section.

Most firmware updates are modifications to the LPU, therefore, the Firmware Revision History for each product will usually reference the LPU Revision History for the detailed changes.

# LPU Revision History

| *LPU Revision* | *Description* |
|---|---|
| | *In general, the greater revision number will contain all the changes made in all lesser revision numbers. There are some exceptions to this, as some features were implemented in parallel and combined in a later revision. Every effort has been made to note these special cases, but be aware that this list may not document all such cases!* |
| 3.21 | Full MIL-STD-1553 product release (this is the final version of the IP-1553 product). This is the baseline firmware version for all subsequent LPU versions. The full set of features are defined in other user manuals. |
| 3.40 | Release of PCI-1553, cPCI-1553, PMC-1553, ISA-1553, PCCARD-1553, IP-D1553, VME/VXI-1553 and QPMC-1553.<br>• Support release of new board product: IP-D1553 (replaces two IP-1553 modules).<br>• Add MIL-STD-1553A capability.<br>• Add auto-Increment time tag register capability.<br>• Adds RT Monitor capability.<br>• Power up in transformer coupled mode (default).<br>• Add improved error injection/detection.<br>• A high word count may now be injected on an RT-RT message. |
| 3.70 | Release of PCI-1553, cPCI-1553, PMC-1553, ISA-1553, PCCARD-1553, IP-D1553, VME/VXI-1553, QPMC-1553 and QPCI-1553.<br>• Support release of new board product: QPCI-1553.<br>• Unified coupling selection across all board models.<br>• LRU Test Bus usage forces direct coupling.<br>• 1553 Voltage DAC powers on at full voltage.<br>• Add Hardwire RT Address capability to QPCI-1553, QPMC-1553.<br>• Add discretes and differential trigger limited capability to QPCI-1553, QPMC-1553<br>• Add RS-485 Functionality to QPCI-1553, QPMC-1553.<br>• Add IRIG determination by API to QPCI-1553, QPMC-1553.<br>• Add Digital IRIG to PCCARD-1553.<br>• Add ability to re-trigger Bus Monitor. |
| 3.80 | Release of IP-D1553, PCCARD-1553, Q104-1553, QPCI-1553, QPMC-1553, QVME-1553 and VME-1553.<br>• Support release of new board products: Q104-1553 and QVME-1553.<br>• Complete discretes and differential trigger capability for QPCI-1553, QPMC-1553, Q104-1553 and QVME-1553.<br>• Full Hardwire RT Address capability for QPCI-1553, QPMC-1553, Q104-1553 and QVME-1553.<br>• Add LRU Test Bus and external LRU connection to the test bus on QPCI-1553.<br>• Meet MIL-STD-1760 boot response requirements for QPCI-1553, QPMC-1553, Q104-1553 and QVME-1553.<br>• Allow host to directly read Tag Time Register.<br>• Add BIT Test for single mode boards. |
| 3.81 | Release of QPMC-1553 to add PCI bursting. |
| 3.84 | Release of IP-D1553, PCCARD-1553, Q104-1553, QPCI-1553, QPMC-1553, QVME-1553, VME-1553, PCI-1553, PMC-1553, CPCI-1553, ISA-1553.<br>• Support Bus Monitor Trigger functionality.<br>• IP-D1553 models, no longer have bus traffic upon reset.<br>• Add PCI 66MHz to QPMC-1553.<br>• Add PCI bursting to QPMC-1553 and QVME-1553. |

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| 3.88, 3.88b1, 3.88b4, 3.88b6, 3.88b7 | Release of IP-D1553, PCCARD-1553, Q104-1553, QPCI-1553, QPMC-1553, QVME-1553, VME-1553, PCI-1553, PMC-1553, CPCI-1553, ISA-1553, PCCARD-D1553.<br>• Support release of new board product: PCCARD-D1553.<br>• Q104-1553P boards now support PCI INTB, INTC and INTD.<br>• Q104-1553 (ISA) boards don't respond to PCI accesses.<br>• Add WCS revision register (not on cPCI-1553, PCI-1553, PMC-1553, ISA-1553).<br>• Add WCS Heartbeat Reg (not on cPCI-1553, PCI-1553, PMC-1553, ISA-1553).<br>• Add Build # to LPU revision.<br>• Add ability to select hardware interrupts for BC.<br>• Time-tag 32-bit reads now use multi-word read.<br>• The "Config Done" LED of QVME-1553 now agrees with the user manual.<br>• Add ability to program Playback bit count error. |
| 3.89 | Support release of new board product: QcP-1553. |
| 3.91 | PCC-D1553 product release with 1553 decoder enhancements. |
| 3.93b97, 3.93b99, 3.93b102 | Release of all MIL-STD-1553 products (except the PCI-1553, PMC-1553, cPCI-1553, and ISA-1553 model legacy boards).<br>• Add a "long cable" test where the BC is able to detect a missed command word "BC no-see" (not on PCI/PMC/cPCI/ISA-1553 model boards).<br>• Fix issues with Hardwire RT Address (inversion/power-on/API initialization).<br>• IRIG Day-of-Year offset of 1 day and IRIG Internal generation year rollover fixed.<br>• QcP-1553 and QVME-1553 decoder enhancements. |
| 3.94b0 | Release of QPMC-1553 for 33MHz PCI, equivalent to 3.93 release of other boards. |
| 3.94b6 | QPCI-1553 release to correct an offset of 10 ms in the IRIG decoder. |
| 3.96b0 | QPMC-1553 release to modify the PCI parity. |
| 4.00b2 | Release of new board product: QPM-1553. All configurations except those that are conduction cooled and/or vibration qualified.<br>• Add the capabilities register and configuration data to flash memory.<br>• Extend the capabilities register to accommodate new options.<br>• Add the ability to interrupt on an Input Trigger.<br>• Store time tag in BC Message Buffer & Stop Buffer (no API support).<br>• Ability to read Minor Frame Time Register (no API support).<br>• Add Playback Abort feature.<br>• Improved error detection capability for RT-RT messages.<br>• Improved BC Overflow message detection algorithm to allow greater bandwidth. |
| 4.11b13, 4.11b15 | Release of AMC-1553, IP-D1553, PCC-D1553, Q104-1553, QCP-1553, QPCI-1553, QPCX-1553, QPM-1553, QPMC-1553, QVME-1553.<br>• Support release of new board product: QPCX-1553.<br>• Extended firmware Version/Build numbers to two 16-bit registers.<br>• Add the capabilities register and configuration data to flash memory.<br>• Extend the capabilities register to accommodate new options.<br>• Add the ability to interrupt on an Input Trigger.<br>• Store time tag in BC Message Buffer & Stop Buffer.<br>• API can now read Minor Frame Time Register.<br>• Add Playback Abort feature. |
| 4.14b2 | Release of QcP-1553.<br>• Changed the CONFIG DONE LED to power up green. |
| 4.19b4 | Release of Q104-1553-P, QcP-1553 and QPCI-1553.<br>• Add the option of monitoring invalid commands, which allows the Bus Monitor and Bus Controller to store message status, command word and time tag for command words with bit or sync errors or for undefined mode codes. |
| 420b1 | Initial product release of QPMC-1553. |

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| | • Assertion of the PCI-Reset signal is no longer honored. |
| 4.20b4 | Initial R15-EC (ExpressCard 1553) product release. |
| 4.21b2 | Release of QcP-1553.<br>• Host interface registers are mapped to each channel (instead of only channel 1).<br>• Assertion of the PCI-Reset signal is no longer honored.<br>• Add enable PCI Reset bit to allow the software to reset the logic.<br>• IRIG no longer has a 10ms offset.<br>• BIT Pass & BIT fail (green & red) LEDs were previously swapped.<br>• BC timing: 2nd frame doesn't start 25 us early. |
| 4.23b4 | Release of 4-channel QVME-1553 (full QVME-1553 release is 4.27b2).<br>• Add System-Reset-Enable.<br>• Add ability for software to read response time-out/late response register. |
| 4.24b1, 4.24b12, 4.24b14 | Release of new product: R15-AMC (Build 12). In addition, Build 1 was the release of the AR-15 MIL-STD-1553 board for a SBC. |
| 4.26b3 | Release of QPMC-1553 for NGC E2 program and for GD Canada.<br>• Disconnecting the 1553 cable while the transmitter is active can cause the error to be reported on the alternate bus – this was corrected. |
| 4.27B2 | Release of QVME-1553.<br>• The "float fix" for configuration & interrupt. |
| 4.40b29, 4.40b30, 4.40b31 | Brings all MIL-STD-1553 boards to the same level (last done with the 4.11 release): IP-D1553-M, IP-D1553-MM, IP-D1553-S, IP-D1553-SS, PCC-D1553, Q104-1553, Q104-1553-2, Q104P-1553, Q104P-1553-2, QcP-1553, QcP-1553-2, QPCI-1553, QPCX-1553, QPM-1553, QPMC-1553, QVME-1553, QVME-1553-2, R15-AMC, R15-EC, RQVME2-1553.<br>• Add Fixed Message Timing Option, which selects the message Gap Time measured from start of successive messages, so that message timing is independent of responses.<br>• Add "Monitor Invalid Command" option, which allows the Bus Monitor and Bus Controller to store message status, command word and time tag for command words with bit or sync errors or for undefined mode codes (4.19b4).<br>• Add "Undefined Mode Code is Illegal" option. Previously, the board would not store Undefined Mode Codes, but now the customer may select to store and respond as illegal mode code.<br>• Firmware no longer clears Dynamic Bus Control Ack in status word upon inputting a receive command.<br>• All PCI & QVME boards now have System-Reset-Enable.<br>• All boards now have the ability for software to read response time-out/late response register.<br>• Several modifications to error injection and message status reporting (4.24b12).<br>• RT suppresses its' data when ME bit is set on a Transmit Last Command mode code (4.24b12).<br>• Corrected an issue when the bus cable was disconnected (4.26b3).<br>• Gap Time for a retry on Busy is now 8 us for both RT's of an RT-RT message.<br>• Fixed a playback issue present in V4.21.<br>• Modified the rate of the heartbeat register (4.24b12).<br>• Fixed a hardwired RT issue (4.24b12). |
| 4.41b4 | Update the AMC-1553 to the v4.40 level and add the HALT command. |
| 4.42b1 | Release of QPCI-1553 to correct an issue with IRIG end of year rollover. |
| 4.46b1, 4.46b2 | Release of Q104-1553.<br>• Add weak pull-up assignments to FPGA (ISA).<br>• Add support of the PCI memory read line instruction (PCI).<br>• Build 2 is only for 2-channel PCI board to fix a synthesis issue on Build 1. |
| 4.51b1, | Release of RPCIe-1553 (4.51b1) and RXMC -1553 (4.51b9). |

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| 4.51b9 | • Update to PCIe host interface (RPCIe-1553) and builds on 4.49 and 4.50 Betas. |
| 4.53 | RPCIe-1553 release.<br>• Addresses an issue only seen on certain models of Dell servers. Expansion ROM accesses were not being serviced, causing system issues when the BIOS attempted to read expansion ROM during boot. |
| 4.55b6 | Release of QPMC-1553.<br>• Enhancements to BC Aperiodics:<br>  ○ NOP is no longer required at the end of an aperiodic list.<br>  ○ All messages occurring near the minor frame tick are recorded.<br>• Add the BC Halt feature (created for AMC-1553 in V4.41).<br>• An issue with IRIG end of year rollover was corrected (V4.42).<br>• Add support of the PCI memory read line instruction.<br>• Once set, Two-Bus status bit now turns off with the following message.<br>• Messages retry properly when message scheduling is used. |
| 4.56b2 | Release of QPMC-1553.<br>• Further modifications to aperiodic messages. |
| 4.62 | Beta release of QVME-1553 board.<br>• Add Flash Write Protect capability. |
| 4.64b2, 4.64b3 | Release of QPM-1553 (4.64b2) and QcP-1553 (4.64b3).<br>• Add ability to get Built-In-Test mode command data from the message buffer.<br>• Incorporate all firmware changes made since V4.40:<br>  ○ Add BC Halt feature.<br>  ○ Add ability to clear the discrete outputs on BC Halt execution.<br>  ○ IRIG end of year rollover was corrected.<br>  ○ Add support of the PCI memory read line instruction.<br>  ○ Once set, Two-Bus status bit now turns off with the following message.<br>  ○ Messages retry properly when message scheduling is used.<br>  ○ Aperiodics: All messages occurring near the minor frame tick are recorded. |
| 4.66b1, 4.66b111 | Release of QcP-1553 (4.66b1), QPCX-1553 (4.66b1) and QPMC-1553 (4.66b111).<br>• Fixes the issue with IRIG disconnection/reconnection.<br>• Add all the changes of V4.64. |
| 4.68b1, 4.68b2 | Release of QPM-1553 (4.68b1 – Beta only for Boeing) and QPCI-1553 (4.68b2).<br>• Fixes an issue with the PCI_target. |
| 5.00b1, 5.00b3 | Initial V5 release of QPM-1553 (5.00b1) and RXMC2-1553 (5.00b3).<br>The highlights of V5 are:<br>• A single RT (sRT) mode will pass RT Validation.<br>• Bus Monitor may run concurrently with single RT.<br>• Add a 32-bit, 1 us resolution Minor Frame Timer option (V4 has 16-bit, 25 us).<br>• Extended 24-bit message gap option (V4 has 16-bit).<br>• Improved the minimum intermessage gap time.<br>• Support for Frame Start Timing mode.<br>• Support flash configuration bits to program the MIL-STD-1553A and the Direct-Coupled control registers at Power-up.<br>• Created a Bus Tester as an internal verification tool used to perform RT validation on Abaco System boards.<br>• Add a noise filter to 1553 input stream for improved noise immunity.<br>• Support zero-crossing early or late injection at 6.25 ns resolution across the complete message.<br>• Support any half-bit (500 ns) sync encoding (error injection).<br>• Support message length (word count errors) error injection for all cases, including appending extra words following a transmit command word.<br>• Support Bi-Phase high and Bi-Phase low in any of the 16 bits or in the parity bit. |

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| | • Low-Bit count is always reported as a Mid-bit error and the Low-Bit count status bit is no longer supported.<br>• sRT meets Mil-Std-1760 Power-on timing and RT Validation power-on test.<br>• BC now stores the data for RT-RT messages.<br>• Improved Mil-Std-1553 Bandwidth using Minor Frame Overflow algorithm.<br>• RT-RT with Transmitting RT with Busy bit set, the receiving RT returns correct status.<br>• Inject Sync, Mid-bit or PE in the transmit command word of an RT-RT message and it treats it as a receive command.<br>• Security bit is readable.<br>• High words input for receive commands are not stored.<br>• RT has 800 us fail-safe time-out.<br>• Single function replaced with dual-function operation: BC/BM or RT/BM.<br>• Add Extended Status Word capability.<br>• Add mixed MIL-STD-1553A/MIL-STD-1553B capability.<br>• Created the RT-RT message format Error bit.<br>• All modifications and bug fixes made since the 4.40 release have been incorporated into V5 for all products. |
| 5.02b1 | Release of RXMC-1553.<br>• Adds support for flash-programmable RT Validated mode allowing single RT and BM. Improved noise immunity by adding input noise filter. Adds support for zero-crossing early or late injection 6.25 ns resolution across the complete message. Adds support for any half-bit (500 ns) sync encoding (error injection). |
| 5.06b14 | Initial release of LPCIe-1553. |
| 5.10b1 | Release of QPM-1553. V5.10 productized the QPM-1553 for Raytheon. |
| 5.14 | Release of RQVME2-1553 Beta. |
| 5.18b28 | Release of QPM-1553, QPCX-1553, R15-LPCIe, RXMC-1553 and QVME-1553-2. This release resolves outstanding issues, supersedes all earlier V5 versions and is the final V5 release. |
| 6.02B7 | First general release of V6 firmware.<br>• The presence of I/O options such as triggers, discrete I/O, differential I/O, digital I/O are reported in a uniform manner using newly defined registers.<br>• The firmware for each product and for the LPU IP used by the product, now have separately maintained revision numbers.<br>• All data paths, registers, and memory pointers are 32 bits wide.<br>• Time tag changed to 64-bits with nanosecond resolution.<br>• Modifications to host interface improve concurrent software support.<br>• The memory map was reorganized: BC, BM, RT and interrupt queue buffer structures were modified.<br>  ○ Multiple BC data buffers (linked list) support added.<br>  ○ BM buffer entries are variable length with a header and byte count to improve memory usage and BM data transfer efficiency.<br>  ○ The Interrupt Queue now has two 32-bit words for each entry instead of three 16-bit words and the queue is a circular buffer.<br>• Added minor frame overflow interrupt.<br>• Control register and playback control register were made thread-safe.<br>• BC_busy bit set on minor frame overflow.<br>• BC low priority frame overflow detection added.<br>• BC high priority frame overflow detection added.<br>• BM overflow interrupt added.<br>• BM trigger is the same interrupt entry as the BM message but with a unique code.<br>• Fixed a bug with power-on busy response in MIL-STD-1553A.<br>• Fixed single RT response at power-up with invalid parity. |

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| | • Fixed a bug with aperiodic lists.<br>• If the BUSY bit is set in the transmitting RT of an RT-RT (or broadcast RT-RT) message, then the Receiving RT will return No Response (RT).<br>• Set the BCR bit in extended status mode, 1553A and mixed mode.<br>• If a mode code or broadcast mode code and the UUT is RT mode (not BM not BC) AND an initiate self-test or reset RT mode code is in process, then the SELF TEST and RESETRT bits will NOT be set in the interrupt status word.<br>• Added global time reset and SMP lock registers. |
| 6.03B10 | Second general release of V6 firmware.<br>• Fixed BC conditional block bug.<br>• For BC Conditional, Noop and Stop message control blocks, stored the next message pointer into the Data Buffer.<br>• Fixed BC aperiodic messages with Frame Start Timing (BC).<br>• Fix to retries with Message Scheduling (BC).<br>• Fixed a bug when retries are enabled but there are no retries (BC mode).<br>• Added the ability for Bus Monitor interrupts to posted in the interrupt queue and not generate hardware interrupts.<br>• For BC Conditional and Timed-Noop message control blocks, updated the time tag register so that the current time is stored.<br>• Fixed a bug when the first of the three Run bits (BC, BM or RT) was turned on during the middle of receiving a MIL-STD-1553 message. This could cause BM interrupts to be inhibited.<br>• Fixed a bug with Conditional/Stop message control blocks when following a NOOP at the start of frame when using retries.<br>• Fixed BM trigger Stop-Trigger (BM mode).<br>• Fixed BM trigger on message status bits (BM mode).<br>• Fixed BM Trigger when message buffer wraps (BM mode).<br>• Fixed BM Trigger counts for multiple events on the same message (BM mode) |
| 6.04B5 | Release for a specific customer: not a general release.<br>• Addressed potential issues when simultaneously running multiple bus controllers on the same bus. This change is not incorporated into firmware versions moving forward.<br>• Software-generated external output trigger is now a minimum of 50 us. |
| 6.05B2 | General release of V6 firmware incorporated into multiple products (based on 6.03B10).<br>• Software-generated external output trigger is now a minimum of 50 us.<br>• The last BC message block of an aperiodic list may now be a STOP control block or a NOOP control block.<br>• Adds the ability to enable/disable the message following a Timed NOOP.<br>• Software-generated external output trigger is now a minimum of 50 us. |
| 6.08B4 | • Gives the ability to retry the message following a NOOP control block. |
| 6.09B4 | • Allow the first message of a frame to be a NOOP control block while running multiple-message aperiodic lists. Previous firmware versions under these conditions would occasionally post an invalid BC Message Pointer location in the interrupt queue. |
| 6.11B1 | • If the application code isn't fast enough to keep up with Bus Monitor real-time operation then data will be lost, BM overflow interrupts will occur, and the application must then re-sync the message buffer pointer to become functional again. When multiple BM overflow interrupts occurred in LPU firmware versions 6.03 through 6.09 the interrupt type was not always updated, so it could appear as an RT, BC or BM interrupt, causing the pointer to be out of range and posting a "515" API error. In a properly designed system, the Bus Monitor should never overflow, and this situation wouldn't occur; however, if it did then the RT software should ignore out-of-range messages. 6.11 firmware updates the interrupt type to the correct code if BM overflows were to occur.<br>• Fixed BC aperiodic messages with Frame Start Timing (BC). There was a bug with V6.03 |

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| | firmware which would cause an additional periodic buslist to transmit within a single frame. It could occur when multiple aperiodic lists are processed before the periodic list is completed. |
| 6.15B1 | • Add ability to generate early zero-crossing at 25, 50, 75 & 100 ns in the MIL-STD-1553 encoder module. |
| 6.17B9 | • Frame Start Timing will always wait for the time programmed in the message block, referenced to the start of frame time, before transmitting the 1553 command word.<br>• Modify the LPU logic to use a synchronous reset rather than an asynchronous reset. |
| 6.17B10 | • Fixed an issue in which the RT did not respond with busy following broadcast commands. |

# Board Product Revision Histories

## AMC-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.11b13 | - | Initial product release. See description in LPU Revision History. |
| 4.41b4 | - | See description in LPU Revision History. |

## IP-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.21 | - | See description in LPU Revision History. |

## IP-D1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.40 | - | See description in LPU Revision History. |
| 3.70 | - | See description in LPU Revision History. |
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b4 | - | See description in LPU Revision History. |
| 3.93b97 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.40b29 | - | General v4.40 release.  1 channel. See description in LPU Revision History. |
| 4.40b31 | - | General v4.40 release.  2 channel. See description in LPU Revision History. |

## ISA-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.40 | - | See description in LPU Revision History. |
| 3.70 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88 | - | See description in LPU Revision History. |

## PCCARD-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.40 | - | See description in LPU Revision History. |
| 3.70 | - | See description in LPU Revision History. |
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |

# PCCARD-D1553 / RPCC-D1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.88 | - | See description in LPU Revision History. |
| 3.91 | - | See description in LPU Revision History. |
| 3.93b97 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.40b41 | - | See description in LPU Revision History. |

# PCI-1553/PMC-1553/cPCI-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.40 | - | See description in LPU Revision History. |
| 3.70 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b1 | - | See description in LPU Revision History. |

# Q104-1553 (ISA 2 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b4 | - | See description in LPU Revision History. |
| 3.88b7 | - | See description in LPU Revision History. |
| 3.93b102 | - | See description in LPU Revision History. |
| 4.11b15 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.40b31 | - | See description in LPU Revision History. |
| 4.46b1 | - | See description in LPU Revision History. |

# Q104-1553 (ISA 4 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b4 | - | See description in LPU Revision History. |
| 3.88b7 | - | See description in LPU Revision History. |
| 3.93b102 | - | See description in LPU Revision History. |
| 4.11b15 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.46b1 | - | See description in LPU Revision History. |

# Q104P-1553 (PCI 2 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b4 | - | See description in LPU Revision History. |
| 3.88b7 | - | See description in LPU Revision History. |
| 3.93b102 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.19b4 | - | See description in LPU Revision History.<br>Q104-1553-2SP is a special build for a single customer. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.46b2 | - | See description in LPU Revision History. |
| 7 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 9 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |

# Q104P-1553 (PCI 4 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b4 | - | See description in LPU Revision History. |
| 3.88b7 | - | See description in LPU Revision History. |
| 3.93b102 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.19b4 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.46b1 | - | See description in LPU Revision History. |
| 4.47b4 | - | Release of Q104-1553-4SPRW. Allows pre-programmed messages for 1760 power-up response, for single customer. Not a formal release. |
| 18 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 20 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 21 | 6.11B1 | See description in LPU Revision History. Beta Version. |

# QCP-1553 (2 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.89 | - | See description in LPU Revision History. |
| 3.93b99 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.14b2 | - | See description in LPU Revision History. |
| 4.19b4 | - | See description in LPU Revision History. |
| 4.21b2 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.64b3 | - | See description in LPU Revision History. |
| 4.66b1 | - | See description in LPU Revision History. |
| 10 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 12 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |

# QCP-1553 (4 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.93b99 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.14b2 | - | See description in LPU Revision History. |
| 4.19b4 | - | See description in LPU Revision History. |
| 4.21b2 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.64b3 | - | See description in LPU Revision History. |
| 4.66b1 | - | See description in LPU Revision History. |
| 28 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 30 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 34 | 6.04B5 | Addressed potential issues when simultaneously running multiple bus controllers on the same bus.<br>See description in LPU Revision History. |
| 35 | 6.04B7 | For BAE San Antonio only.<br>Adds ability to detect high word when BC is ignoring extenal traffic. |
| 38 | 6.03B10 | Fixed potential initialization issue by updating the SDC file to include timing for the PLX IC and the RAM. |

# QPCI-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.70 | - | See description in LPU Revision History. |
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b6 | - | See description in LPU Revision History. |
| 3.88b7 | - | See description in LPU Revision History. |
| 3.93b97 | - | See description in LPU Revision History. |
| 3.94b6 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.19b4 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.42b1 | - | See description in LPU Revision History. |
| 4.68b2 | - | See description in LPU Revision History. |

## QPCX-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.11b13 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.66b1 | - | See description in LPU Revision History. |
| 5.18b28 | - | See description in LPU Revision History. |
| 26 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 36 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |

## QPMC-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.40 | - | See description in LPU Revision History. |
| 3.50 | - | Unreleased beta for three channel board for a single customer. |
| 3.70 | - | See description in LPU Revision History. |
| 3.80 | - | See description in LPU Revision History. |
| 3.81 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b7 | - | See description in LPU Revision History. |
| 3.94b0 | - | See description in LPU Revision History. |
| 3.94b2 | - | See description in LPU Revision History. |
| 3.96b0 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 420b1 | - | See description in LPU Revision History. |
| 4.22b36 | - | Release of a special configuration of QPMC-1553-2MCQ4 for a single customer. |
| 4.26b3 | - | “Disconnect issue”<br>Scott McCarthy at GD Canada discovered a problem with the BC NoSee error when disconnecting the 1553 cable. The problem shows up when a cable is disconnected, and the board is set up to switch to the alternate bus. If the BC’s transmitter is active when a cable is disconnected then a BC NoSee error is detected on Bus A, but is not correctly cleared in some cases when switching to Bus B and gets posted as an error on the message on bus B<br>See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.55b6 | - | See description in LPU Revision History. |
| 4.56b2 | - | See description in LPU Revision History. |
| 4.66b111 | - | See description in LPU Revision History. |

## QPM-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.00b2 | - | Initial product release. See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 4.64b2 | - | See description in LPU Revision History. |
| 4.68b1 | - | See description in LPU Revision History. |
| 5.00b1 | - | See description in LPU Revision History. |
| 5.10b1 | - | See description in LPU Revision History. |
| 5.18b28 | - | See description in LPU Revision History. |
| 26 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 36 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 52 | 6.05B2 | Beta release |
| 58 | 6.08B3 | See description in LPU Revision History. |
| 103 | 6.17B10 | 2-channel hardware / firmware adaption with pin-out change for specific customer. |

## QVME-1553 (2 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b6 | - | See description in LPU Revision History. |
| 3.93b99 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.27b3 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 5.18b28 | - | See description in LPU Revision History. |

## QVME-1553 (4 channel) Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |
| 3.88b6 | - | See description in LPU Revision History. |
| 3.93b99 | - | See description in LPU Revision History. |
| 4.11b13 | - | See description in LPU Revision History. |
| 4.23b4 | - | See description in LPU Revision History. |
| 4.27b3 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |

## R15-AMC Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.24B12 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |

## R15-EC Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.20b4 | - | See description in LPU Revision History. |
| 4.40b29 | - | See description in LPU Revision History. |
| 21 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 23 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |

## R15-LPCIE Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 5.06b14 | - | See description in LPU Revision History. |
| 5.18b28 | - | See description in LPU Revision History. |
| 13 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 16 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |

## R15-MPCIE Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 1 | 6.09B4 | Initial release. See description in LPU Revision History. |

## R15-USB & R15-USB-MON Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 173 | 6.02B7 | Initial firmware release for R15-USB.<br>Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 174 | 6.03B4 | Released as beta.<br>This fixes a bug in rev 173 firmware in which some bad data can appear at the beginning of the bus monitor queue when the BM is started while there is live bus traffic. |
| 176 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 177 | 6.05B2 | Released as beta; adds 1PPS option on IRIG output.<br>See description in LPU Revision History. |
| 191 | 6.11B1 | Initial firmware release for R15-USB-MON |

## RAR15XF Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 149 | 6.03B10 | Initial release<br>See description in LPU Revision History. |
| 203 | 6.09B4 | See description in LPU Revision History. |

## RAR15-XMC-IT Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 148 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 156 | 6.03B4 | See description in LPU Revision History. |
| 163 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 164 | 6.05B1 | Beta |
| 165 | 6.06B1 | See description in LPU Revision History. |
| 167 | 6.07B1 | NGC only.<br>See description in LPU Revision History. |
| 200 | 6.05B2 | Beta for GEAS VCP only - includes forced reconfiguration addition. |
| 201 | 6.05B2 | Corrects reported ARINC channel types. |
| 203 | 6.09B4 | See description in LPU Revision History. |
| 204 | 6.09B4 | Added ARINC receiver flush capability. No 1553 modificaitons. |
| 208 | 6.17b10 | • Updated LPU to 6.17b10 which fixes a problem with startup busy response following a broadcast command.<br>• Read completions will not be started on the upstream if buffers are not available.<br>• Fixed the reset polarity on the PCI_ENGINE module and included other reset changes in compliance with the DO-254 certification process.<br>• Added a circuit to detect the case where the link does not come up for approximately 3.355 seconds. When that condition is detected, a re- |

| | | |
|---|---|---|
| | | configuration is forced. This condition was encountered with the TB3-TO-CMC-LP expansion chassis during "hot-swap" (the link did not complete training and was stuck in the initial link detect LTSSM state). |
| 209 | 6.17b10 | Changed the SMBus master module to conform with the DO-254 certification process. |

## RPCIE-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.51b1 | - | See description in LPU Revision History. |
| 4.53 | - | See description in LPU Revision History. |
| 20 | 6.02B3 | |
| 21 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 23 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 24 | 6.05B2 | Beta release. Addresses an issue with the timing of timed NOOP commands executed by the bus controller.<br>See description in LPU Revision History. |
| 26 | 6.08B4 | Addresses an issue where expansion ROM accesses are not being serviced. The issue manifests as the system hanging during boot when the BIOS attempts to read expansion ROM. This issue was seen on certain models of Dell servers.<br>See description in LPU Revision History. |

## RQVME2-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.40b30 | - | See description in LPU Revision History. |
| 4.40b32 | - | See description in LPU Revision History. |

## RXMC-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 4.51b9 | - | See description in LPU Revision History. |
| 5.02b1 | - | See description in LPU Revision History. |
| 5.18b28 | - | See description in LPU Revision History. |
| 22 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 24 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 28 | 6.08B4 | Beta release. Adds support for I/O option 7.<br>See description in LPU Revision History. |
| 30 | 6.09B4 | See description in LPU Revision History. |

## RXMC2-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 20 | 6.02B7 | Part of the general release with LPU 6.02B7.<br>See description in LPU Revision History. |
| 22 | 6.03B10 | Part of the general release with LPU 6.03B10.<br>See description in LPU Revision History. |
| 23 | 6.11B01 | Beta release. See description in LPU Revision History. |
| 24 | 6.15B1 | See description in LPU Revision History. |
| 29 | 6.17B9 | See description in LPU Revision History. |

## VME-1553 / VXI-1553 Firmware Revision History

| *Firmware Revision* | *LPU Revision* | *Description* |
|---|---|---|
| 3.40 | - | See description in LPU Revision History. |
| 3.80 | - | See description in LPU Revision History. |
| 3.84 | - | See description in LPU Revision History. |