Hardware Reference Manual

MIL-STD-1553 Hardware Installation and Reference Manual

Publication No. 1500-046 Rev. A

Supporting Products:

- AMC-1553
- PCCARD-D1553
- Q104-1553
- Q104-1553P
- QCP-1553
- QPCI-1553
- QPCX-1553
- QPM-1553
- QPM-1553-TB
- QPMC-1553
- QVME-1553
- QVXI2-1553X
- R15-AMC
- R15-EC
- R15-LPCIE
- R15-MPCIE
- R15-USB
- RAR15-XMC-IT
- RAR15XF
- RAR15XF-TB
- RPCC-D1553
- RPCIE-1553
- RQVME2-1553
- RXMC-1553
- RXMC-1553-TB
- RXMC2-1553
- CABLES

abaco SYSTEMS

Document History

Revision	Date	Description
A	12/04/19	ECN 20098982
6.13	04/23/19	Fixed three hyperlinks and added more specific information to Thunderbolt™ 3 product variants.
6.12	04/02/19	Added Thunderbolt™ 3 product variants.
6.11	02/12/19	Added cable length information to the various cable descriptions in Appendix A. Removed appendix chapter A.13 titled “CONM50-D25-1 Transition Cable” as it is not referenced in this manual and renumbered the remaining appendix chapters including figures and tables. Updated R15-MPCIE Molex and Omnetics connector information. Updated section A.10 cable description.
6.10	10/09/18	Added I/O specifications for all cards. For the RXMC-1553, added P16-F1 and -F2. Changed 28V_DISC max power source from 48V to 43V. Added “28V Discrete I/O” section. For the R15-EC, corrected P1 pin numbers. Updated Q104 P1 pin table to show shared External RT addressing names. For USB-1553, added Avionics Discretes section 17.8. Removed R15-USB-MON section as it has its own manual. Removed IP-D1553, VME-1553 and VXI-1553 products as they have been discontinued and are no longer supported by the API. QVXI-1553X has been replaced by the QVIXI2-1553X. Updated Figure 6-1 to remove GE Fanuc symbol. Updated Figures 16-1 and 16-2 with latest Abaco branding. Added Appendix A and removed transition cable info from the individual card sections as they now appear in Appendix A. Updated Table 1-1.
6.09	01/31/18	Modified the BusTools/1553-API installation destination folders
6.07	03/13/17	Updated section 21.5 to indicate that R15-LPCIE dedicated output triggers are low true.
6.06	11/10/16	Added chapter 20 for the R15-MPCIE and rebranded for Abaco.
6.00	11/12/13	Added a new chapter for the RAR15XF (chapter 19).
5.01	07/01/12	RXMC2-1553 updated in Table 3 to have V6 firmware available. Table 56, pin 58 changed from EXT_RST+/DIS10 to EXT_RST-/DIS10. In Table 2, RAR15-XMC dedicated trigger inputs changed from 2 to 4. Updated the Trigger section of the Q104-1553-P, QCP, QPM, QPCX, R15-USB, RAR15-XMC, R15-LPCIE, RPCIE-1553 and R15-EC. Table 2, changed R15-LPCIE Avionics discretes from 10 to 12.
5.00	06/24/12	Initial release.

Waste Electrical and Electronic Equipment (WEEE) Returns

Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

About This Manual

Conventions

Notices

This manual may use the following types of notice:

WARNING

Warnings alert you to the risk of severe personal injury.

CAUTION

Cautions alert you to system danger or loss of data.

NOTE

Notes call attention to important features or instructions.

TIP

Tips give guidance on procedures that may be tackled in a number of ways.

LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” as well as “+” and “-“ denote the low and high components of a differential signal respectively.

Further Information

Abaco Website

You can find information regarding Abaco products on the following website:

LINK

https://www.abaco.com

Abaco Documents

This document and other reference documentation is distributed via the Abaco website. You may register for access to manuals via the website.

LINK

https://www.abaco.com/products/avionics

Third-party Documents

NOTE

Technical literature describing components used on the Abaco products is available from the manufacturers' websites.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

Technical Support Contact Information

You can find technical assistance contact details on the website Support page.

LINK
https://www.abaco.com/support

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:

LINK
support@abaco.com

Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Support page.

LINK
https://www.abaco.com/support

Do not return products without first contacting the Abaco Repairs facility.

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1 • Introduction

This manual describes the hardware and software installation of Abaco's MIL-STD-1553 products listed on the front cover. These high-performance MIL-STD-1553 interface boards offer a wide range of options, providing compatibility with almost any system.

This chapter provides an overview of this manual and includes a series of tables which summarize the maximum I/O capabilities for each board. The board's I/O and features may vary, depending on its configuration and firmware version.

A general software installation procedure is outlined in Chapter 2 "BusTools/1553-API Installation Quick Start". The remaining chapters, except for the last one, are card-specific. They cover additional software installation instructions, hardware installation (if applicable), board features and connector pin assignments.

Chapter 20 "Interface Signals" provides descriptions of the various I/O signals. Where applicable, it also describes how the latest V6 firmware provides enhanced I/O features over the previous firmware releases. This last chapter should be used as a reference for the I/O products identified in the individual board chapters. I/O details not outlined in the individual board chapters are provided in the "Interface Signals" chapter.

Appendix A provides a section for each available transition cable for cards in this manual. In most cases, pictures are provided as well as connector components and cable pin assignments. A board to transition cable cross-reference is also provided at the beginning of the appendix.

Additionally, the latest product information including downloads such as datasheets, application notes, software and user manuals can be found on the Abaco website listed below.

LINK
https://www.abaco.com

Table 1-1 Product Environmental Characteristics / Options

Product Name	Form Factor	Notes	Comm. Temp.	Ext. Temp.	Cond. Cooled	RoHS
AMC-1553	AMC			•		
PCCARD-D1553	PCMCIA		•	•		
Q104-1553	PC104	ISA	•	•		
Q104-1553-P	PC104 Plus	PCI				
QCP-1553	CPCI	3U, PCI or PXI	•			
QPM-1553	PMC		•	•	•	
QPM-1553-TB	Thunderbolt 3	Thunderbolt 3	•			
QPMC-1553	PMC		•	•	•	
QPCI-1553	PCI					
QPCX-1553	PCI		•	•		
QVME	VME		•	•	•	
QVXI2-1553X	VME	6U, VXI	•	•		•
R15-AMC	AMC		•	•		•
R15-EC	Express Card		•	•		•
R15-LPCIE	PCIE	1 Lane, Low Profile		•	•	•
R15-MPCIE	PCIE	1 Lane		•	•	•
R15-USB	USB			•		•
RAR15-XMC	XMC	1-Lane				•
RAR15XF	XMC	1-Lane	•			•
RAR15XF-TB	Thunderbolt 3	Thunderbolt 3	•			•
RPCC-D1553	PCMCIA	Newer Version of PCCARD-D1553	•	•		
RPCIE-1553	PCIE	4 Lane				•
RQVME2-1553	VME	6U	•	•		•
RXMC-1553	XMC	1 Lane		•	•	•
RXMC-1553-TB	Thunderbolt 3	Thunderbolt 3	•			•
RXMC2-1553	XMC	4 Lane	•	•	•	

Table 1-2 Product Max I/O Features Summary

Product Name	MIL-STD-1553 Channels	ARINC Available	Variable Voltage	Software Selectable Coupling	LRU Bus	Test Bus	IRIG Input	IRIG Output	Avionics Discretes	Differential I/O	PIO (Serial TTL I/O)	Dedicated Trigger Inputs	Dedicate4d Trigger Outputs	Ext RT Addr. Shared with Disc	Dedicated Ext RT Addr.
AMC-1553	4						•	•	18			1		2	
PCCARD-D1553	2						•	•	2			1	1		
Q104-1553	4						•	•	10	2		1	1	1	
Q104-1553-P	4								10	2		1	1	1	
QCP-1553	4		•	•			•	•	18	2				2	
QPM-1553(-TB)	4		•	•			•	•	18	8		1		2	
QPMC-1553	4		•	•			•	•	18	8		1	1	2	
QPCI-1553	4			•					10	2				1	
QPCX-1553	4		•	•	•	•	•	•	10	2				1	
QVME	4			•			•	•	4			4	4		4
QVXI2-1553X	4		•		•		•	•	4			4	4		4
R15-AMC	4						•	•				1		2	
R15-EC	2						•	•	2			1	1		
R15-LPCIE	2		•	•			•	•	12	2		2	2		1
R15-MPCIE	2						•	•	2	1					1
R15-USB	2						•	•	8						
RAR15-XMC	4	•		•			SE	•	12	2		4			1
RAR15XF(-TB)	4	•		•			•	•	12	2				1	
RPCC-D1553	2						•	•	2			1	1		
RPCIE-1553	4		•				•	•	18			1		2	
RQVME2-1553	4		•		•		•	•	4			4	4		4
RXMC-1553(-TB)	2						•	•	12	4	8	2			2
RXMC2-1553	4		•	•			•	•	12	2		4			

NOTE

IRIG input is differential unless identified as SE for single-ended.

Table 1-3 Notes and V6 Firmware Availability

Product Name	I/O Notes	Pre V6 Notes	V6 F/W Available
AMC-1553	Trigger is Diff.		
PCCARD-D1553			
Q104-1553		RS485_0 is dedicated trig in. RS485_1 is dedicated trig out.	
Q104-1553-P		RS485_0 is dedicated trig in. RS485_1 is dedicated trig out.	•
QCP-1553	Dedicated 1 diff in and 1 diff out.		•
QPM-1553(-TB)	Diffs tradeoff for Disc. Trigger is Diff.		•
QPMC-1553			
QPCI-1553			
QPCX-1553			•
QVME	Ext RT Addr on P2 Conn.		
QVXI2-1553X	No rear IO.		
R15-AMC			
R15-EC			•
R15-LPCIE			•
R15-MPCIE	2 External LED outputs		•
R15-USB			•
RAR15-XMC	The IRIG input can also be the one PPS input signal. The IRIG output can also be the one PPS output signal.	Flash-based RT offset. Diff dedicated inputs for a clock and a time-tag reset.	•
RAR15XF(-TB)			•
RPCC-D1553			
RPCIE-1553			•
RQVME2-1553	Ext RT Addr on P2 Conn.		
RXMC-1553(-TB)	Discretes can replace 4ch of open/ground with 28v/open.	Flash-based RT offset.	•
RXMC2-1553		Flash-based RT offset. Diff dedicated inputs for a clock and a time-tag reset.	•

2 • BusTools/1553-API Installation Quick Start

2.1 Before You Begin

The BusTools/1553-API software supports Abaco's MIL-STD-1553 product line listed on the front cover. This Quick Start provides general installation steps for these products and target operating systems.

NOTE

For VxWorks, Integrity, QNX and LynxOS installation, refer to the appropriate chapter in the "BusTools/1553-API User's Manual" provided with the product or also available on the Abaco website.

NOTE

For Thunderbolt 3 products, please refer to the "TB3-TO-CMC-LP Thunderbolt™ 3 Expansion Adapter User's Guide" provided with the product or also available on the Abaco website. This document contains important additional information for operating in a Thunderbolt environment.

All PCI, PMC and *CompactPCI* Bus products running on Windows, Linux and Solaris are Plug'N' Play and have resources assigned by the system at startup.

For ISA Bus boards (PCCARD-D1553, RPCC-D1553 and Q104-1553), a memory region and IRQ need to be assigned. To avoid conflicts with other ISA devices, make sure the factory default range in the table below is open.

Board Type	Memory Region
PCCARD-D1553 RPCC-D1553	0xD0000 – 0xD1FFF
Q104-1553	0xD0000 – 0xD3FFF

If the memory range conflicts with another device, select a different range. See the particular product's chapter in this manual for installation instructions for setting another base memory address. Check the resources on the system for available memory and IRQ. Provide the base address and IRQ number for ISA boards during installation.

2.2 BusTools/1553-API Installation

2.2.1 32- and 64-Bit Windows

Administrative rights are required to install the BusTools/1553-API software package.

To install the software, perform the following steps:

1. Install the software first!
2. Exit all programs.

3. Insert the BusTools/1553-API installation CD-ROM.
4. The installation program launches automatically when the CD is inserted into the drive. If it does not, double-click the file SETUP.EXE located in the SETUP subdirectory of the BusTools/1553-API CD-ROM.
5. Follow the installation procedure. Make sure the correct Hardware Platform and the Board Type are selected.
6. Upon completing the software installation, power down the system and follow the Hardware Installation Instructions for the Abaco board being installed.

2.2.2 Multiple Card Installations [Windows]

For multiple card installations, begin by installing the API as above. After powering down the system, insert the first card in the system and power up. Once the system configures the device driver for the first card, the drivers for each successive board may be installed by launching the Setup program once for each additional device. Continue successive API installations and subsequent card additions until all cards are in the system and configured, then power cycle the system to complete the setup.

2.2.3 Linux and Solaris

Root privileges are required to install the device driver, BusTools/1553-API library and example programs.

1. Install the hardware first!
2. Insert the BusTools/1553-API installation CD and copy the installation files from the CD, located in the “Linux” or “Solaris” install directory in compressed tar format.
3. Extract the files under /root/Condor_Engineering. If the directory does not exist, create it.
4. For Linux, run the install script in /root/Condor_Engineering/Install.
5. For Solaris, run the install script in the ./Condor_Engineering/MIL-STD-1553/Driver directory.
6. Detailed descriptions of the installation are in the install READMEs in the installation directory on the CD.

2.2.4 Multiple Card Installations [Non-Windows Systems]

For multiple card installations, insert all cards into the system. Power up the system and complete the software installation as detailed above.

2.3 Hardware Installation

All hardware devices are static-sensitive. Before handling any hardware device, attach the static strap provided to the metal chassis of the system. Make sure that the

system is plugged into a grounded outlet and turned off. Insert the hardware device into an appropriate slot and secure it with a screw on the end panel mounting plate.

2.4 PCI, PCIe, PMC, XMC and CompactPCI Device Driver Installation

The Windows Device Manager detects new hardware upon startup and configures the driver for the board.

2.4.1 32-Bit and 64-Bit Windows

All 32-Bit and 64-Bit Windows operating systems (except Windows NT) have a Device Manager.

1. Once the system is restarted, after installing the BusTools/1553-API Software, the Windows Device Manager should automatically install the driver.

LINK

https://www.abaco.com/embedded-support

2. If the *New Hardware Found* dialog box appears upon starting the system, follow the on-screen instructions to install the device driver.

NOTE

For Window NT, skip the driver installation and go directly to step 3.

3. Test the installation by running **QuikView1553**. A QuikView1553 icon will be added to the desktop. QuikView1553 can also be run from the Start menu.

2.4.2 Linux and Solaris

The install script automically installs the device driver and builds the API library and example programs. Test the installation by running the tstall or tst_bc example programs in the ./Examples directory.

The driver will need to be reloaded if the system is powered down. See the UNIX chapter of the “BusTools/1553-API User’s Manual” provided with the product or also available on the Abaco website for instructions for re-installing the driver.

3 • QPCI-1553 and QPCX-1553 Installation

3.1 QPCI-1553 and QPCX Installation Procedure

This section explains how to install the QPCI-1553 and QPCX-1553 boards. The QPCI-1553 / QPCX-1553 are single-, dual- or quad-channel 1553 interface boards supporting universal PCI signaling. The main difference between the two is that the newer QPCX supports the 66MHz PCI bus. With API version 5.64 and newer, the two boards are drop-in replaceable. Prior to API version 5.64, the QPCX will work but will not support hardware interrupts.

NOTE

The QPCI-1553 has been discontinued.

NOTE

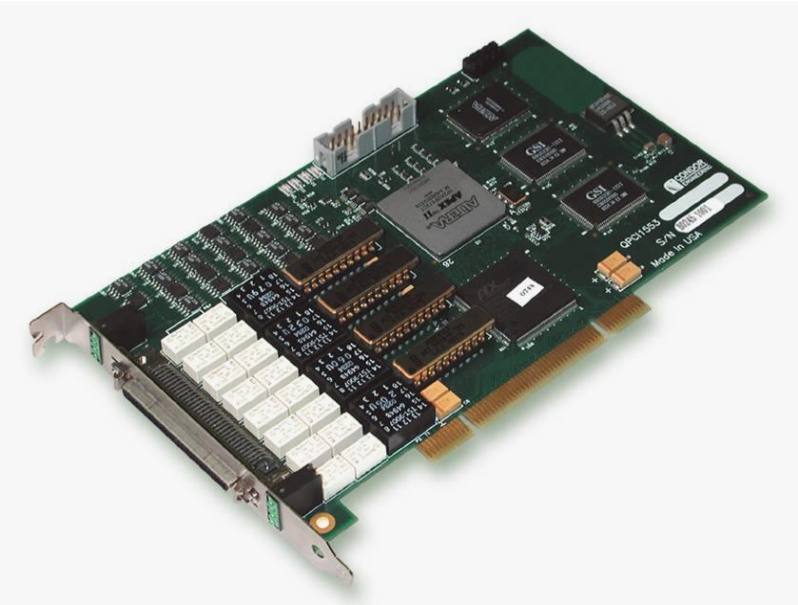
There are differences in the 1553 shields between the two boards as described in this chapter.

3.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Remove the cover from the PC. Remove the mounting plate from one of the unused PCI slots in the computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
3. Connect a transition cable assembly to the board to make the required MIL-STD-1553 bus and various I/O connections.

3.2 QPCI-1553 Board Layout

Figure 3-1 QPCI-1553



3.3 QPCX-1553 Board Layout

Figure 3-2 QPCX-1553

3.4 Status LEDs

There are eight LEDs on the mounting plate of the QPCI-1553 / QPCX-1553:

- **CH 1, CH 2, CH 3, CH 4 – 1553 Bus Activity -** The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic.
- **INIT DONE, INIT ERR – Configuration Status** – INIT DONE illuminates green on successful FPGA configuration; INIT ERR illuminates green on failed FPGA configuration. The QPCI-1553 / QPCX-1553 configures from an onboard configuration device, so the INIT DONE LED should be illuminated under normal conditions.
- **BIT PASS, BIT FAIL** – **Built-In-Test (BIT) Status –** These LEDs can be controlled by the Application or user. BIT PASS illuminates green on successful BIT; BIT FAIL illuminates red on failed BIT. Both LEDs are off before the first BIT attempt.
- There are four bi-colored status LEDs on the top (component side) of the QPCI-1553 / QPCX-1553:
- **B0, B1, B2, B3 LEDs – 1553 Bus Activity** – Labeled D1 – D4 respectively on the PCB, the status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).
- There are two additional bi-colored status LEDs on the top (component side) of the QPCX-1553:
- **LED3 – CPLD Configuration** –Green indicates CPLD configuration loaded whereas red indicates a load failure.
- **LED4 – Power Good** –Green indicates onboard 1.2 V & 2.5 V supplies are within tolerance and red indicates there is an out of tolerance condition.

3.5 QPCI-1553 / QPCX-1553 Connector Description

3.5.1 QPCI-1553 / QPCX-1553 I/O Connector

The QPCI-1553 / QPCX-1553 use a single 68-pin SCSI connector (P1) on the mounting plate for all I/O. The pinout is specified in the following table.

Table 3-1 QPCI-1553 / QPCX-1553 Front Panel Pin Assignments

Pin	Function	Pin	Function
1	1553 CH1A+	35	ADISC7
2	1553 CH 1A-	36	ADISC8
3	1553 CH 1A Shield*	37	ADISC9
4	GND	38	ADISC10
5	1553 CH 1B+	39	485/422 CH1+
6	1553 CH 1B-	40	485/422 CH1-
7	1553 CH 1B Shield	41	GND
8	RTADDR1_0/ADISC1	42	EXT CLK+/Trigger+
9	RTADDR1_1/ADISC2	43	EXT CLK-/Trigger-
10	1553 CH 2A+	44	GND
11	1553 CH 2A-	45	GND
12	1553 CH 2A Shield*	46	GND
13	GND	47	LRUA Shield (QPCI only)*
14	1553 CH 2B+	48	LRUA+
15	1553 CH 2B-	49	LRUA -
16	1553 CH 2B Shield*	50	GND
17	RTADDR1_2/ADISC3	51	IRIGB IN
18	RTADDR1_3/ ADISC4	52	IRIGB OUT
19	1553 CH 3A+	53	IRIGB IN Return
20	1553 CH 3A-	54	GND
21	1553 CH 3A Shield*	55	-
22	GND	56	-
23	1553 CH 3B+	57	-
24	1553 CH 3B-	58	GND
25	1553 CH 3B Shield*	59	LRUB+
26	-	60	LRUB -
27	GND	61	LRUB Shield (QPCI only)*
28	1553 CH 4A+	62	-
29	1553 CH 4A-	63	GND

Pin	Function
30	1553 CH 4A Shield*
31	GND
32	1553 CH 4B+
33	1553 CH 4B-
34	1553 CH 4B Shield*

Pin	Function
64	RTADDR1_4/ADISC5
65	RTADDR1_P/ ADISC6
66	-
67	-
68	GND

NOTE

For the QPCI, the LRUx Shield signals are tied to their respective transformer secondary center taps. On the QPCX, these signals do not exist and are open.

NOTE

Forthe QPCI, the individual 1553 Shields are tied to their respective transformer secondary center taps. For the QPCX, the transformer secondary center taps are not connected. However, to provide backward compatibility to the QPCI, the QPCX can be ordered with these signals tied to their respective transformer secondary center taps.

3.5.2 QPCI-1553 / QPCX-1553 Transition Cables

Separate Transition Cable assemblies are provided with one-, two- and four-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONQPMC-X section.

3.6 MIL-STD-1553B Signals

The 1553 CH *n*A/B SHIELD is tied to the center tap of the isolation transformer of the respective bus on the QPCI-1553 board. These signals are only connected on the QPCX-1553 by special order.

3.7 LRU Port Connection

The QPCI-1553 / QPCX-1553 provide a transformer-coupled stub connection available for a Line Replaceable Unit (LRU) device under test. One or more channels can be attached on the QPCI-1553 / QPCX-1553 card to the onboard Test Bus and communicate with the external LRU device over this port. In this mode, an external LRU TX-coupled device is attached to this connection without requiring external coupling transformers or terminators, as those are provided by the card's Test Bus.

LRUA+ and LRUA- are the differential pair for bus A. LRUB+ and LRUB- are the differential pair for bus B.

LRUA/B SHIELD tie to the center taps of the isolation transformers for the LRU Port on the QPCI-1553 board. These signals are not connected on the QPCX-1553 board.

3.8 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
QPCI & QPCX
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
QPCI
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

QPCX
Voh_max = 5.25 V - Zout drop
Voh_min = 3.8 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma.
Iol / Ioh = 16 mA max
Zout = 10 Ω output series resistance.

3.9 Avionics Discrete I/O

The QPCI-1553 / QPCX-1553 have ten discrete I/O signals (ADISC X) available on the interface connector, six of which are optionally shared with the first channel's Hardwire RT functionality.

Output specs:
Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:
Input range -0.5 to 43 V max.

QPCI
Input interally pulled to 3.3 V via 22 KΩ after input protection diode
Vil = -0.5 V to 2.5 V
Vih = 2.8 V to 43 V

QPCX
Input interally pulled to 3.3 V via 10 KΩ after input protection diode
Vil = -0.5 V to 1.9 V
Vih = 2.2 V to 43 V.

3.10 Hardwired RT Address

Hardwired RT Addressing on the first channel is available and is enabled by installing a shunt across JP1 and using ADISC1- ADISC6 for RTADD1_0 - RTADD1_5 and RTADD1_P respectively.

3.11 Triggers

3.11.1 Pre-V6 Firmware

One differential trigger input and one differential trigger output is available. For the QPCX only, they can be used single-ended as well since the negative terminal is biased at ~ 1.8V.

QPCI
Output specs:
Vod (differential) = 2 V min into 50 Ω load, 5 V max.
Voc (common mode) = 3 V max.

Input specs:
Vth (diff threshold) = ±0.2 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 1000 uA max @ Vin = 12 V, -800 uA max @ Vin = -7 V
Rin = 12 KΩ min

QPCX
Output specs:
Vod (differential) = 1.8 V min into 54 Ω load, 5 V max.
Voc (common mode) = 2.9 V max.

Input specs:
Vth (diff threshold) = ±0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 500 uA max @ Vin = 12 V, -400 uA max @ Vin = -7 V
Iin = 1000 uA max @ Vin = 25 V, -800 uA max @ Vin = -20 V
Rin = 24 KΩ min not taking into account Vneg_bias resistors.

Negative pin bias:
Vneg_bias = ~1.8 V via 10 KΩ pull-up to 3.3V and 13 KΩ pull-down to ground.

3.11.2 V6 Firmware, QPCX Only

Any Avionics discrete or differential can be programmed as a trigger input and output on a per-channel basis. The specifications are the same as for pre-V6 firmare.

3.12 Memory Map Info

The QPCI-1553 / QPCX-1553 map into an 8-MB address block (BAR2). The BIOS maps the 1553 board into memory space at an address above the total amount of

RAM in the computer. The QPCI-1553 uses a 128-byte PCI configuration space for the PLX (BAR0); whereas, the QPCX-1553 uses a 512-byte space. The QPCI also allocates a 128-byte PLX I/O space which is required but not actually used (BAR1); whereas, the QPCX allocates a 256-byte space. Direct access to these registers is not available through the API.

4 • QCP-1553 Installation

4.1 QCP-1553 Installation Procedure

This section explains how to install the QCP-1553 board. The QCP-1553 is a single-, dual- or quad-channel 1553 interface board with universal PCI signaling in a *CompactPCI* form factor.

NOTE

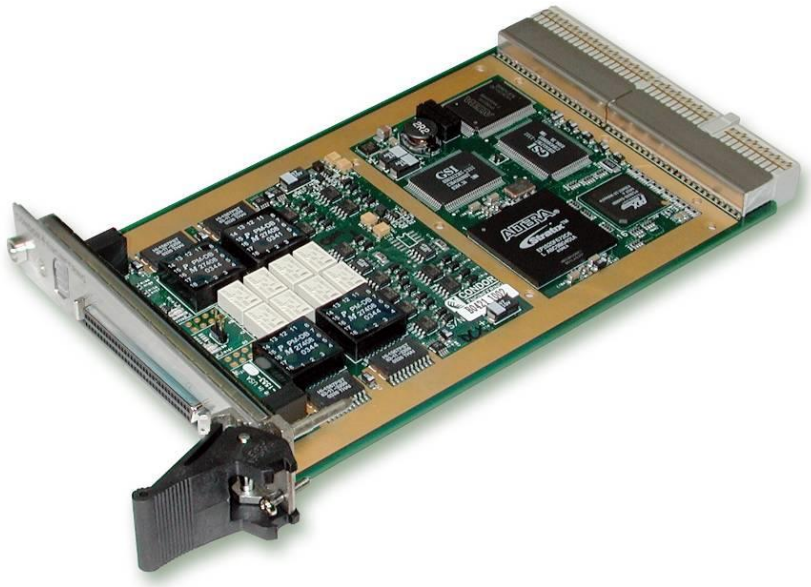
The QCP-1553 has been discontinued.

4.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Install the board in an available slot in the *CompactPCI* system, securing the card with the faceplate's captive screw.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with the board.

4.2 QCP-1553 Board Layout

Figure 4-1 QCP-1553



4.3 Status LEDs

There are eight bi-colored status LEDs on the front panel of the QCP-1553, in addition to several on the circuit board surface:

- **D1 [A-D] - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when detecting 1553 bus traffic, and it illuminates orange if that channel runs internally (transceiver transmit inhibited). Channel is silk-screened on the faceplate.
- **D2 [A-D]** – As noted on the faceplate silkscreen, one green LED for FPGA Configuration Done, one green LED for Host Activity and a Bi-Color LED for BIT. The QCP-1553 configures from an onboard configuration device, so the CONFIG LED should be illuminated shortly after powerup under normal conditions. This LED lights red briefly prior to configuration, then lights green after successful configuration. This LED can be controlled by the Application or user. It illuminates green for successful BIT and red for BIT fail. The LED is not illuminated until after BIT attempt.
- **D5** – Config Done is also provided on the board surface for boards built without front panel status indicators, e.g. Conductive-Cooled boards.

4.4 QCP-1553 Connector Description

4.4.1 QCP-1553 Front Panel I/O Connector

The QCP-1553 uses a single 68-pin SCSI connector (P1) on the mounting plate for all I/O. The front panel pinout is specified in the following table.

Table 4-1 QCP-1553 Front Panel Pin Assignments

Pin	Function	Pin	Function
1	1553 CH 1A+	35	ADISC7
2	1553 CH 1A-	36	ADISC8
3	1553 CH 1 Shield	37	RTADDR2_0/ADISC9
4	GND (for ADISC1)	38	RTADDR2_1/ADISC10
5	1553 CH 1B+	39	485+ OUT
6	1553 CH 1B-	40	485- OUT
7	1553 CH 1 Shield	41	485 Shield
8	RTADDR1_0/ADISC1	42	485+ IN
9	RTADDR1_1/ADISC2	43	485- IN
10	1553 CH 2A+	44	RTADDR2_2/ADISC11
11	1553 CH 2A-	45	RTADDR2_3/ADISC12
12	1553 CH 2 Shield	46	GND (for ADISC5)
13	GND (for ADISC2)	47	GND
14	1553 CH 2B+	48	-
15	1553 CH 2B-	49	-

Pin	Function
16	1553 CH 2 Shield
17	RTADDR1_2/ADISC3
18	RTADDR1_3/ ADISC4
19	1553 CH 3A+
20	1553 CH 3A-
21	1553 CH 3 Shield
22	GND
23	1553 CH 3B+
24	1553 CH 3B-
25	1553 CH 3 Shield
26	HW_RT
27	GND
28	1553 CH 4A+
29	1553 CH 4A-
30	1553 CH 4 Shield
31	GND (for ADISC3)
32	1553 CH 4B+
33	1553 CH 4B-
34	1553 CH 4 Shield

Pin	Function
50	GND (for ADISC7)
51	IRIGB IN
52	IRIGB OUT
53	IRIGB IN Return
54	GND (for ADISC8)
55	RTADDR2_4/ADISC13
56	RTADDR2_p/ADISC14
57	ADISC15
58	ADISC16
59	-
60	-
61	GND
62	ADISC17
63	ADISC18
64	RTADDR1_4/ADISC5
65	RTADDR1_P/ ADISC6
66	-
67	-
68	GND (overall Shield)

4.4.2 QCP-1553 Transition Cable

Separate Transition Cable assemblies are provided with one-, two- and four-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONQPMC-X section.

4.4.3 QCP-1553 Rear I/O Pinout

Rear I/O (Order Option) pinout is specified in the following table.

Table 4-2 QCP-1553 Rear I/O Pin Assignments

Pin	Function
A1	1553 CH 1A+
A2	1553 CH 1A-
B2	1553 CH 1 Shield
B1	GND
C2	1553 CH 1B+
C1	1553 CH 1B-
D2	1553 CH 1 Shield
A3	RTADDR1_0/ADISC1
C3	RTADDR1_1/ADISC2

Pin	Function
A4	ADISC7
B4	ADISC8
A7	RTADDR2_0/ADISC9
C7	RTADDR2_1/ADISC10
C11	485+ OUT
D11	485- OUT
E11	485 Shield
E12	485+ IN
E10	485- IN

Pin	Function
A5	1553 CH 2A+
A6	1553 CH 2A-
B3	GND
B6	1553 CH 2 Shield
B7	GND
C6	1553 CH 2B+
C5	1553 CH 2B-
D5	1553 CH 2 Shield
D3	RTADDR1_2/ADISC3
E3	RTADDR1_3/ ADISC4
A9	1553 CH 3A+
A10	1553 CH 3A-
B10	1553 CH 3 Shield
D10	GND
C10	1553 CH 3B+
C9	1553 CH 3B-
D9	1553 CH 3 Shield
D1	HW_RT_En [rear I/O option]
D4	GND
A13	1553 CH 4A+
A14	1553 CH 4A-
B14	1553 CH 4 Shield
D14	GND
C14	1553 CH 4B+
C13	1553 CH 4B-
D13	1553 CH 4 Shield

Pin	Function
D7	RTADDR2_2/ADISC11
E7	RTADDR2_3/ADISC12
B5	GND
B9	GND
B11	GND
B13	GND
B15	GND
B17	GND
E8	IRIGB IN
C8	IRIGB OUT
B8	IRIGB IN Return
	-
E6	RTADDR2_4/ADISC13
E5	RTADDR2_P/ADISC14
A12	ADISC15
A11	ADISC16
D6	GND
D8	GND
D12	GND
B12	ADISC17
C12	ADISC18
E2	RTADDR1_4/ADISC5
E1	RTADDR1_P/ ADISC6
D16	GND
D18	GND
D20	GND

4.5 MIL-STD-1553B Signals

The 1553 CH *n*A/B SHIELD is tied to the center tap of the isolation transformer of the respective channel on the QCP-1553 board.

4.6 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

4.7 Avionics Discrete I/O

Eighteen discrete I/O signals are available, twelve of which can be optionally shared with the first two channels' Hardwire RT functionality.

Output specs:
Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:
Input interally pulled to 3.3 V via 22 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.5 V
Vih = 2.8 V to 43 V

4.8 Hardwired RT Address

Hardwired RT Addressing is available on the first two channels and is shared with the Avionics Discretes. This operational mode is enabled by installing a shunt across JB1, grounding P1-26 **or** grounding
J2-D1 on rear I/O models only.

4.9 Triggers

4.9.1 Pre-V6 Firmware

One differential trigger input and one differential trigger output are available.

Output specs:
Vod (differential) = 2 V min into 50 Ω load, 5 V max.
Voc (common mode) = 3 V max.

Input specs:
Vth (diff threshold) = ±0.3 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 500 uA max @ Vin = 12 V, -500 uA max @ Vin = -7 V
Rin = 22 KΩ min

4.9.2 V6 Firmware

Any Avionics discrete or differential 485_IN can be programmed as a trigger input on a per-channel basis. Any Avionics discrete or differential 485_OUT can be programmed as a trigger output on a per-channel basis.

4.10 Memory Map Info

The QCP-1553 maps into an 8-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer. Additionally, the QCP-1553 maps a 512-byte memory region for PCI local control and another 256-byte region in I/O space. The board also has a 128-byte PCI configuration register. Direct access to these regions is not available through the API.

5 • QPM-1553 and QPMC-1553 Installation

NOTE

The QPMC-1553 has been discontinued.

NOTE

If you purchased the QPM-1553-TB variant of this product, please also refer to the "TB3-TO-CMC-LP Thunderbolt™ 3 Expansion Adapter User's Guide" provided with the product or also available on the Abaco website (https://www.abaco.com/TB3LP_Guide). This document contains important additional information for operating in a Thunderbolt environment.

5.1 QPM-1553 and QPMC-1553 Installation Procedure

This section explains how to install the QPM-1553 and QPMC-1553 boards. The QPM-1553 and QPMC-1553 are single-, dual- or quad-channel 1553 interface boards developed to the PMC specification. The QPM-1553 integrates several devices on the QPMC-1553 with the latest technology components, but otherwise, is a direct replacement to the QPMC-1553. This document may henceforth use the term "QPM-1553 / QPMC-1553" in place of the term "QPM-1553 and QPMC-1553".

5.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Mount the QPM-1553 / QPMC-1553 to the carrier using the hardware provided.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with the board (Front Panel version only.)

5.2 QPM-1553 Board Layout

Figure 5-1 QPM-1553

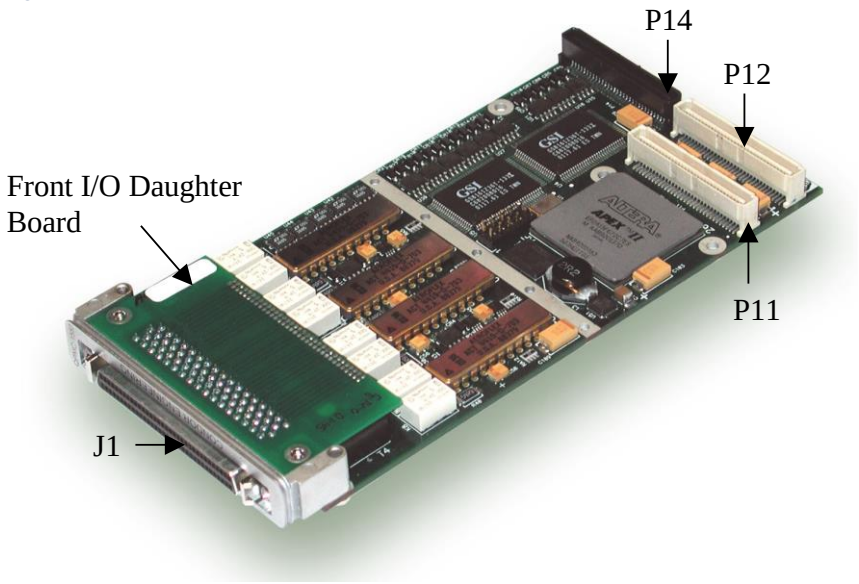
5.2.1 QPM-1553 Status LEDs

There are seven bi-colored status LEDs on the backside of the QPM-1553:

- **Bus 1 (D1), Bus 2 (D2), Bus 3 (D3) and Bus 4 (D4) LEDs - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).
- **FPGA CFG OK LED (D5) – Configuration Status** – Red prior to FPGA configuration. Green on successful FPGA configuration.
- **BIT PASS, BIT FAIL (D6)** – **BIT Status –** These LEDs can be controlled by the Application or user. BIT PASS illuminates green on successful BIT; BIT FAIL illuminates red on failed BIT. Both LEDs are off before the first BIT attempt.
- **FLASH LED (D7) –** Green with valid 3.3 V power for configuration programmable logic device. Flashes red briefly prior to FPGA configuration.

5.3 QPMC-1553 Board Layout

Figure 5-2 QPMC-1553



5.3.1 QPMC-1553 Status LEDs

There are six bi-colored status LEDs on the backside of the QPMC-1553:

- **B0, B1, B2, B3 LEDs - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).
- **CFG OK LED – Configuration Status** – Red prior to FPGA configuration. Green upon successful FPGA configuration.
- **BIT PASS, BIT FAIL (D6)** – **BIT Status –** These LEDs can be controlled by the Application or user. BIT PASS illuminates green on successful BIT; BIT FAIL illuminates red on failed BIT. Both LEDs are off before the first BIT attempt.

5.4 QPM-1553 and QPMC-1553 Connector Description

The QPM-1553 / QPMC-1553 are designed to PCI Specification 2.2. The PCI bus logic signals route through connectors P11 and P12.

The QPM-1553 / QPMC-1553 use a daughter board with a 68-pin SCSI connector (J1) on the front panel I/O version. The I/O signals are routed to P14 for the rear-panel I/O versions.

5.4.1 QPM-1553 / QPMC-1553 P14 Pin Assignments

Table 5-1 below specifies the rear panel connector pin assignments for both the standard and -H build options.

Table 5-1 QPM-1553 / QPMC-1553 P14 Pin Assignments

Pin	STD Function	-H Function	Pin	STD Function	-H Function
1	RTADDR2_P/ADISC14	485_CH6-	2	RTADDR1_P/ADISC6	RTADDR1_P/ ADISC6
3	GND	GND	4	RTADDR1_4/ADISC5	RTADDR1_4/ ADISC5
5	ADISC15	485_CH7+	6	RTADDR1_3/ADISC4	RTADDR1_3/ ADISC4
7	--	485_CH1+	8	--	485_CH1-
9	ADISC16	485_CH7-	10	~HWRT_EN	~HWRT_EN
11	--	485_CH2+	12	--	485_CH2-
13	ADISC17	485_CH8+	14	RTADDR1_2/ADISC3	RTADDR1_2/ ADISC3
15	GND	GND	16	1553 CH2A-	1553 CH2A-
17	ADISC1	485_CH8-	18	1553 CH2A+	1553 CH2A+
19	GND	GND	20	1553 Shield*	1553 Shield*
21	RTADDR2_4/ADISC13	485_CH6+	22	1553 CH2B-	1553 CH2B-
23	GND	GND	24	1553 CH2B+	1553 CH2B+
25	GND	GND	26	GND	GND
27	1553 CH3B+	1553 CH3B+	28	1553 CH3A-	1553 CH3A-
29	ADISC7/TRIG_0	ADISC7/TRIG_0	30	1553 CH3A+	1553 CH3A+
31	GND	GND	32	1553 CH3B-	1553 CH3B-
33	GND	GND	34	GND	GND
35	ADISC8/TRIG_1	ADISC8/TRIG_1	36	1553 CH1B-	1553 CH1B-
37	GND	GND	38	1553 CH1B+	1553 CH1B+
39	RTADDR2_0/ADISC9	ADISC9	40	GND	GND
41	--	485_CH3+	42	--	485_CH3-
43	RTADDR2_1/ADISC10	ADISC10	44	RTADDR1_1/ADISC2	RTADDR1_1/ ADISC2
45	--	485_CH4+	46	--	485_CH4-
47	RTADDR2_2/ADISC11	485_CH5+	48	RTADDR1_0/ADISC1	RTADDR1_0/ ADISC1
49	GND	GND	50	1553 CH1A-	1553 CH1A-
51	RTADDR2_3/ADISC12	485_CH5-	52	1553 CH1A+	1553 CH1A+
53	IRIGB OUT	IRIGB OUT	54	IRIGB IN	IRIGB IN
55	GND	GND	56	IRIGB IN Return	IRIGB IN Return
57	GND	GND	58	EXT_IN-	EXT_IN-
59	1553 Shield*	1553 Shield*	60	EXT_IN+	EXT_IN+
61	1553 CH4B-	1553 CH4B-	62	1553 CH4A-	1553 CH4A-

Pin	STD Function	-H Function
63	1553 CH4B+	1553 CH4B+

Pin	STD Function	-H Function
64	1553 CH4A+	1553 CH4A+

NOTE

For the QPMC, all of the transformer secondary center taps are tied together and become the signal 1553_Shield. For the QPM, the transformer secondary center taps are not connected. The signal 1553_Shield is tied to the mounting bossess.

5.4.2 QPM-1553 / QPMC-1553 Front Panel Pinout

Table 5-2 below specifies the front panel connector pin assignments for both the standard and -H build options.

Table 5-2 QPM-1553 / QPMC-1553 Front Panel Pin Assignments

Pin	STD Function	-H Function
1	1553 CH1A+	1553 CH1A+
2	1553 CH 1A-	1553 CH 1A-
3	1553 Shield*	1553 Shield*
4	GND	GND
5	1553 CH 1B+	1553 CH 1B+
6	1553 CH 1B-	1553 CH 1B-
7	1553 Shield*	1553 Shield*
8	RTADDR1_0/ADISC1	RTADDR1_0/ ADISC1
9	RTADDR1_1/ADISC2	RTADDR1_1/ ADISC2
10	1553 CH 2A+	1553 CH 2A+
11	1553 CH 2A-	1553 CH 2A-
12	1553 Shield*	1553 Shield*
13	GND	GND
14	1553 CH 2B+	1553 CH 2B+
15	1553 CH 2B-	1553 CH 2B-
16	1553 Shield*	1553 Shield*
17	RTADDR1_2/ADISC3	RTADDR1_2/ ADISC3
18	RTADDR1_3/ADISC4	RTADDR1_3/ ADISC4
19	1553 CH 3A+	1553 CH 3A+
20	1553 CH 3A-	1553 CH 3A-
21	1553 Shield*	1553 Shield*
22	GND	GND
23	1553 CH 3B+	1553 CH 3B+
24	1553 CH 3B-	1553 CH 3B-
25	1553 Shield*	1553 Shield*
26	~HWRT_EN	~HWRT_EN

Pin	STD Function	-H Function
35	ADISC7/TRIG0	ADISC7/TRIG0
36	ADISC7/TRIG1	ADISC8/TRIG1
37	RTADDR2_0/ADISC9	ADISC9
38	RTADDR2_1/ADISC10	ADISC10
39	--	--
40	--	--
41	GND	GND
42	EXT_IN+	EXT_IN+
43	EXT_IN-	EXT_IN-
44	RTADDR2_2/ADISC11	ADISC11
45	RTADDR2_3/ADISC12	ADISC12
46	GND	GND
47	GND	GND
48	--	--
49	--	--
50	GND	GND
51	IRIGB IN	IRIGB IN
52	IRIGB OUT	IRIGB OUT
53	IRIGB IN Return	IRIGB IN Return
54	GND	GND
55	RTADDR2_4/ADISC13	ADISC13
56	RTADDR2_P/ADISC14	ADISC14
57	ADISC15	ADISC15
58	ADISC16	ADISC16
59	--	--
60	--	--

Pin	STD Function	-H Function
27	GND	GND
28	1553 CH 4A+	1553 CH 4A+
29	1553 CH 4A-	1553 CH 4A-
30	1553 Shield*	1553 Shield*
31	GND	GND
32	1553 CH 4B+	1553 CH 4B+
33	1553 CH 4B-	1553 CH 4B-
34	1553 Shield*	1553 Shield*

Pin	STD Function	-H Function
61	GND	GND
62	ADISC17	ADISC17
63	ADISC18	ADISC18
64	RTADDR1_4/ADISC5	RTADDR1_4/ADISC5
65	RTADDR1_P/ADISC6	RTADDR1_P/ADISC6
66	--	--
67	--	--
68	GND	GND

NOTE

For the QPMC, all of the transformer secondary center taps are tied together and become the signal 1553_Shield. For the QPM, the transformer secondary center taps are not connected. The signal 1553_Shield is tied to the mounting bossess.

5.4.3 QPM-1553 / QPMC-1553 Transition Cable

Separate Transition Cable assemblies are provided with one-, two- and four-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONQPMC-X section.

5.5 MIL-STD-1553B Signals

The 1553 SHIELD is tied to the center tap of all the isolation transformers on the QPM-1553 and is tied to Chassis on the QPMC-1553 board.

5.6 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

5.7 Avionics Discrete I/O

Both boards provide eighteen discrete I/O (ADISC X) signals, twelve of which can be optionally shared with the first two channels' Hardwire RT functionality.

For the QPM-1553 –H build, there are only ten discrete I/O signals, six of which can optionally be shared with the first channels' Hardwire RT functionality.

Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:

QPMC
Input interally pulled to 3.3 V via 22 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V

QPM
Input interally pulled to 5 V via 750 Ω after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V.

5.8 Hardwired RT Address

Both boards provide Hardwired RT Addressing on the first two channels. This operational mode is enabled by grounding J1-26 front I/O versions or grounding P14-10 on rear I/O models and using the appropriate Avionics Discrete.

For the QPM-1553 –H build, only the first channel is available for Hardwired RT Addressing.

5.9 Triggers

5.9.1 Pre-V6 Firmware

Both boards include one differential trigger input.

The "**-H**" option (available on QPM-1553 only) includes eight bi-directional differential I/O channels.

Output specs:

Vod (differential) = 2 V min into 50 Ω load, 5 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 500 uA max @ Vin = 12 V, -400 uA max @ Vin = -7 V
Iin = 1000 uA max @ Vin = 25 V, -800 uA max @ Vin = -20 V
Rin = 24 KΩ min not taking into account Vneg_bias resistors.

5.9.2 V6 Firmware, QPM Non-H Version Only

Any Avionics discrete or differential EXT_IN can be programmed as a trigger input on a per-channel basis. Any Avionics discrete can be programmed as a trigger output on a per-channel basis.

5.10 Memory Map Info

Both boards provide require an 8-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

6 • AMC-1553 Installation

6.1 AMC-1553 Installation Procedure

This section explains how to install AMC-1553 boards. The AMC-1553 is a single-, dual- or quad-channel 1553 interface board developed to the AMC specification.

6.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Mount the AMC-1553 board into the chassis or carrier board.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with the board.

The AMC I/O configuration is defined below.

6.2 AMC-1553

Figure 6-1 AMC-1553

NOTE

Front panel assembly not shown in this photograph.

6.3 Status LEDs

There are twelve bi-colored status LEDs on the backside of the AMC-1553:

- **Bus 1 (D1), Bus 2 (D2), Bus 3 (D3) and Bus 4 (D4) LEDs - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic and illuminates red if that channel runs internally (transceiver transmit is inhibited).
- **FPGA CFG OK LED (D5) – Configuration Status** – Red prior to FPGA configuration. Green on successful FPGA configuration.
- **BIT PASS, BIT FAIL (D6)** – **Built-in-test Status –** These LEDs can be controlled by the Application or user. BIT PASS illuminates green on successful BIT; BIT FAIL illuminates red on failed BIT. Both LEDs are off before the first BIT attempt.
- **FLASH LED (D7) –** Green with valid 3.3 V power for configuration programmable logic device. Flashes red briefly prior to FPGA configuration.
- **PCIe LANE GOOD LEDs (DS5-DS8) –** Green if the given PCIe lane in working properly. DS5-DS8 LEDs are for PCIe lanes 1-4 respectively.
- **POWER FAIL LED (DS9) –** Red if a payload power has not been applied to the board. This could indicate a power failure on the board or it could also indicate that the shelf controller has not yet enabled payload power.

6.3.1 On-Board Switches

- **IPMI Configuration Switches (SW2) –** All switches (1-4) should be in the OFF position for normal operation.

6.3.2 AMC-1553 Front Panel Pinout

The front panel connector pin assignment is specified in Table 6-1.

Table 6-1 AMC-1553 Front Panel Pin Assignments

Pin	Signal	Pin	Signal
1	N/C	51	ADISC8/Trigger_1
2	N/C	52	Chassis
3	N/C	53	N/C
4	ADISC6/ RTADD1_P	54	GND
5	N/C	55	N/C
6	ADISC17	56	1553 CH 4A+
7	N/C	57	N/C
8	N/C	58	Chassis
9	N/C	59	N/C
10	ADISC14/ RTADD2_P	60	GND
11	N/C	61	N/C
12	IRIGB RTN	62	1553 CH 3A+

Pin	Signal
13	N/C
14	GND
15	N/C
16	GND
17	N/C
18	ADISC11/ RTADD2_2
19	N/C
20	GND
21	N/C
22	ADISC10/ RTADD2_1
23	N/C
24	ADISC7/Trigger_0
25	N/C
26	N/C
27	N/C
28	N/C
29	N/C
30	N/C
31	N/C
32	ADISC5/ RTADD1_4
33	ADISC18
34	GND
35	N/C
36	ADISC16
37	ADISC15
38	ADISC13/ RTADD2_4
39	GND
40	IRIGB OUT
41	IRIGB IN
42	N/C
43	N/C
44	GND
45	ADISC12/ RTADD2_3
46	TRIG_IN -

Pin	Signal
63	N/C
64	Chassis
65	N/C
66	GND
67	N/C
68	1553 CH 2A+
69	N/C
70	Chassis
71	N/C
72	GND
73	N/C
74	1553 CH1A+
75	N/C
76	N/C
77	N/C
78	N/C
79	1553 CH 4B-
80	1553 CH 4B+
81	Chassis
82	1553 CH 4A-
83	GND
84	~HWRT_EN
85	1553 CH 3B-
86	1553 CH 3B+
87	Chassis
88	1553 CH 3A-
89	ADISC4/ RTADD1_3
90	ADISC3/ RTADD1_2
91	1553 CH 2B-
92	1553 CH 2B+
93	Chassis
94	1553 CH 2A-
95	ADISC2/ RTADD1_1
96	ADISC1/ RTADD1_0

Pin	Signal
47	TRIG_IN+
48	N/C
49	N/C
50	ADISC9/ RTADD2_0

Pin	Signal
97	1553 CH 1B-
98	1553 CH 1B+
99	Chassis
100	1553 CH 1A-

6.3.3 AMC-1553 Transition Cable

Contact Abaco Sales for information regarding availability of the AMC-1553 transition cable.

6.4 MIL-STD-1553B Signals

The 1553 SHIELD is tied to chassis ground and should be used as the overall shield for each differential pair.

6.5 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

6.6 Avionics Discrete I/O

Eighteen discrete I/O signals are provided, twelve of which are optionally shared with the first two channels' Hardwire RT functionality.

Output specs:
Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:
Input interally pulled to 3.3 V via 22 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V

6.7 Hardwired RT Address

Hardwired RT Addressing is available on the first two channels and are shared with the Avionics Discretes.

6.8 Differential Triggers

One differential trigger input is available on the interface connector.

Output specs:

Vod (differential) = 2 V min into 50 Ω load, 5 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 500 uA max @ Vin = 12 V, -400 uA max @ Vin = -7 V
Iin = 1000 uA max @ Vin = 25 V, -800 uA max @ Vin = -20 V
Rin = 24 KΩ min not taking into account Vneg_bias resistors.

6.9 Memory Map Info

The board requires an 8-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

7 • R15-AMC Installation

7.1 R15-AMC Installation Procedure

This chapter explains how to install R15-AMC boards. The R15-AMC is a single-, dual- or quad-channel 1553 interface board developed to the AMC specification and plugs into a PCIe slot.

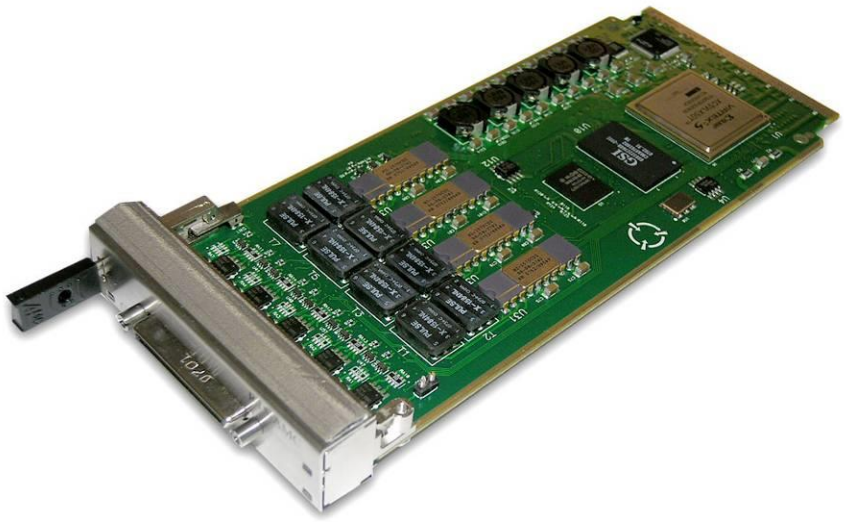
7.1.1 Hardware Installation

4. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
5. Remove the cover from the PC. Remove the mounting plate from one of the unused PCIe slots in the computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
6. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with the board.

The AMC I/O configuration is defined below. A transition cable is provided from the AMC I/O connector to MIL-STD-1553 cable jacks and a D50 connector for other I/O signals.

7.2 R15-AMC

Figure 7-1 R15-AMC



7.3 Status LEDs

There are five status LEDs on the backside of the R15-AMC:

- **Bus 1 (D1), Bus 2 (D2), Bus 3 (D3) and Bus 4 (D4) LEDs - 1553 Bus Activity** – The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic.
- FPGA CFG OK LED (D5) – Configuration Status – Red on successful FPGA configuration.
- In addition, there are three AMC LEDs on the bezel, defined per AMC 2.0 Specification:
- **Blue** – Hot Swap status.
- **Red** (LED 1) – Fault or "Out of Service"
- **Green** (LED 2) – Additional Module Status.

7.3.1 Hot Swap Extract Switch

There is a Hot Swap Extract Switch located on the left side of the front of the bezel. This switch is in conformance with the AMC 2.0 Specification.

7.3.2 R15-AMC Front Panel Pinout

The front panel connector pin assignment is specified in Table 7-1.

Table 7-1 R15-AMC Front Panel Pin Assignments

Pin	Function	Pin	Function
1	1553 CH1A+	35	1553 CH 1A-
2	CHASSIS	36	CHASSIS
3	1553 CH 1B+	37	1553 CH 1B-
4	1553 CH 2A+	38	1553 CH 2A-
5	CHASSIS	39	CHASSIS
6	1553 CH 2B+	40	1553 CH 2B-
7	1553 CH 3A+	41	1553 CH 3A-
8	CHASSIS	42	CHASSIS
9	1553 CH 3B+	43	1553 CH 3B-
10	1553 CH 4A+	44	1553 CH 4A-
11	CHASSIS	45	CHASSIS
12	1553 CH 4B+	46	1553 CH 4B-
13	TRIG_IN+	47	TRIG_IN-
14	DISCRETE1 / RTADDR1_0	48	GND
15	DISCRETE2 / RTADDR1_1	49	GND
16	DISCRETE3 / RTADDR1_2	50	GND
17	DISCRETE4 / RTADDR1_3	51	GND
18	DISCRETE5 / RTADDR1_4	52	GND
19	DISCRETE6 / RTADDR1_P	53	GND

Pin	Function
20	DISCRETE7
21	DISCRETE8
22	DISCRETE9 / RTADDR2_0
23	DISCRETE10 / RTADDR2_1
24	DISCRETE11 / RTADDR2_2
25	DISCRETE12 / RTADDR2_3
26	DISCRETE13 / RTADDR2_4
27	DISCRETE14 / RTADDR2_P
28	DISCRETE15
29	DISCRETE16
30	DISCRETE17
31	DISCRETE18
32	~HWRT_EN
33	IRIGRX_POS
34	IRIGTX

Pin	Function
54	GND
55	GND
56	GND
57	GND
58	GND
59	GND
60	GND
61	GND
62	GND
63	GND
64	GND
65	GND
66	GND
67	IRIGRX_NEG
68	GND

7.3.3 R15-AMC Transition Cable

Contact Abaco Sales for information regarding availability of the R15-AMC transition cable. A pinout of the transition cable is provided in the Appendix A R15-AMC Transition Cable section.

7.4 MIL-STD-1553B Signals

The 1553 SHIELD is tied to chassis ground and should be used as the overall shield for each differential pair.

7.5 IRIG Signaling

IRIG time may be received on the signals IRIGRX_POS and IRIGRX_NEG.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V
Voh_min = 2.2 V min
Vol = 0.4 V max @ 12 ma
Iol / Ioh = 12 mA max
Zout = No output series resistance.

7.6 Avionics Discrete I/O

Eighteen discrete I/O signals are provided, twelve of which can be optionally shared with the first two channels' Hardwire RT functionality.

Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:

REV 1 & REV 2
Input interally pulled to 3.3 V via 10 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 1.65 V
Vih = 1.65 V to 43 V

REV 3
Input interally pulled to 3.3 V via 10 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 1.81 V
Vih = 2.18 V to 43 V

7.7 Hardwired RT Address

Hardwired RT Addressing is available on the first two channels and are shared with the Avionics Discretes.

7.8 Differential Triggers

One differential trigger input is available on the interface connector.

Input specs:

Vth (diff threshold) = $\pm$0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 500 uA max @ Vin = 12 V, -400 uA max @ Vin = -7 V
Iin = 1000 uA max @ Vin = 25 V, -800 uA max @ Vin = -20 V
Rin = 24 KΩ min.

7.9 Memory Map Info

The board requires an 8-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

8 • PCCARD-D1553 / RPCC-D1553 Installation

8.1 Installation Procedure

This section tells how to install the PCCARD-D1553 and RPCC-D1553 PCMCIA boards, both of which support one or two 1553 Channels. The RPCC-D1553 is a newer software-compatible design with an updated enclosure and cables for long-term availability. Unless otherwise indicated in this chapter and throughout this manual, the term RPCC-D1553 applies to both cards.

 NOTE

The PCCARD-D1553 has been discontinued.

8.1.1 Hardware Installation

After installing the software, follow the steps below to install the hardware.

Windows NT 4.0

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag.
2. Turn off the power to the PC and insert the RPCC-D1553 into the PC Card slot.
3. Powerup the computer. The driver should be loaded automatically upon powerup.

32-Bit Windows

1. After installing the software install the RPCC-D1553 and restart the system.

The Windows 98/95 Plug and Play hardware manager should detect new hardware and configure the drivers for the board.

2. When prompted, reboot the computer.

Windows 95

1. If the *New Hardware Found* dialog box doesn't appear when the system starts, select *Add New Hardware* from the Control Panel.
2. If Windows 95 does not automatically detect the device drivers, and a prompt for a path to the driver location appears, enter **C:\Windows\Inf\Other** and click *OK*.

Windows 98

1. When the *Add New Hardware* dialog box detects the new hardware with its corresponding device number next to the hardware device, click *NEXT*.
2. Select *Display a list of all the drivers in a specific location*, select the desired driver. Click NEXT.
3. When the hardware being installed appears in the Models Window, select the device and click *NEXT*.

If nothing appears, go to step 5. Click *NEXT* again.

4. Click *FINISH*, then Click *YES* to reboot.
5. If the *New Hardware Found* dialog box does not appear when the system starts, select *Add New Hardware* from the Control Panel.
6. If the device drivers are not automatically detected, and a prompt for a path to the driver location appears, enter **C:\Windows\Inf\Other** and click *OK*.

Complete Installation for All Operating Systems

1. Connect the supplied transition cable assembly to the board.
2. Connect the MIL-STD-1553 bus to the cable assembly.

The RPCC-D1553 I/O configuration is defined below.

8.2 PCCARD-D1553

Figure 8-1 PCCARD-D1553 Card with Transition Cable

8.3 RPCC-D1553

Figure 8-2 RPCC-D1553 Card with Transition Cable

8.4 RPCC-D1553 Connector Description

The RPCC-D1553/PCCARD-D1553 connector P1 implements the PCMCIA interface and P2 connector mates to the supplied transition cable. Although the RPCC-D1553 uses a different enclosure and mating connector than the PCCARD-D1553, the included cable uses the same pin assignments as the PCCARD-D1553 for user interface compatibility.

8.4.1 RPCC-D1553 Transition Cables

Separate Transition Cable assemblies are provided with one or two-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONPCCD-X section:

8.5 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

8.6 Avionics Discrete I/O

Two discrete I/O pins are available on the D9 connector.

Output specs:

PCCARD-D1553
Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

PPCC-D1553
Open drain output with Vds = 43 V max.
Vol = 0.55 V max @ Iol = 0.5 A, 0.47 V max @ Iol = 100 mA

Input specs:

PCCARD-D1553
Input interally pulled to 3.3 V via 22 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V

RPCC-D1553
Input interally pulled to 3.3 V via 10 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V.

8.7 RPCC-D1553/PCCARD-D1553 Memory Map Info

The RPCC-D1553/PCCARD-D1553 board may be mapped into any available 8-Kbyte block in upper memory between segment addresses A000:0000 and E400:0000 (physical addresses A0000 to E4000 hexadecimal). The memory address is used by Card Services to map the RPCC-D1553/PCCARD-D1553 memory and must not conflict with any other device. The memory is paged by an internal page register, which is accessed in memory space at word offset 0x08 (See the "MIL-STD-1553 Universal Core Architecture Reference Manual" for more information).

NOTES

When using any program to determine if a memory or I/O space is available for use, most only report what the operating system knows. If no operating system driver has been installed for a memory or I/O region, the program might report that it is available, even if some device is really using that region.

If multiple boards are being used in the same platform, then sufficient memory space must be available for each board.

The "Quick Start" installation guide lists specific steps that might assist in determining which upper memory address space is available.

8.8 Interrupt Line Select

The RPCC-D1553/PCCARD-D1553 board features software-programmable interrupt line selection. There are no interrupt jumpers to set. An interrupt (not being used by another board) must be chosen.

The hardware interrupt number is selected when installing the software for 32-Bit Windows. Selecting "0" disables the hardware interrupts; the API defaults to polling the board.

CAUTION

Many PCMCIA controllers do not adequately document their own interrupt routing from the Card, through Card Services, then to the system. Therefore, enabling interrupts without complete knowledge of the system may lead to unexpected conditions.

9 • R15-EC Installation

9.1 Installation Procedure

This section tells how to install the R15-EC board. The R15-EC is an ExpressCard/54 product with one or two 1553 channels.

9.1.1 Hardware Installation

After installing the software, follow the steps below to install the hardware. The R15-EC installs into the ExpressCard/54 slot on the computer. An ExpressCard/54 slot on the host computer is required in order to install the R15-EC.

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Insert the R15-EC into the ExpressCard/54 slot.
3. Connect the supplied transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly. The R15-EC I/O configuration is defined below.

9.2 R15-EC

Figure 9-1 R15-EC Card

9.3 R15-EC Connector Description

9.3.1 R15-EC Front Panel I/O Connector

Table 9-1 R15-EC P1 Connector Pin Assignments

Pin	Signal	Pin	Signal
1	Channel 1 BUS A+	19	Channel 1 BUS A-
2	Do not connect	20	Do not connect
3	Channel 1 BUS B+	21	Channel 1 BUS B-
4	Channel 2 BUS A+	22	Channel 2 BUS A-
5	Ground	23	Do not connect
6	Channel 2 Bus B+	24	Channel 2 Bus B-
7	Do not connect	25	Ground
8	Trigger Input	26	Trigger Output
9	IRIG Output	27	Ground
10	IRIG Input+	28	IRIG Input-
11	Discrete #1	29	Ground
12	Discrete #2	30	Do not connect
13	Do not connect	31	Do not connect
14	Do not connect	32	Do not connect
15	Do not connect	33	Do not connect
16	Do not connect	34	Do not connect
17	Do not connect	35	Do not connect
18	Do not connect	36	Do not connect

NOTE

The connector on the R15-EC is AMP/Tyco, P/N 2-5178238-5 or equivalent. Any compatible mating connector may be used.

9.3.2 R15-EC Transition Cables

Separate Transition Cable assemblies are provided with one and two-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONR15-EC-X section.

9.4 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 KΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.45 V max + Zout drop @ 4 ma
Iol / Ioh = 4 mA max
Zout = 49.9 Ω output series resistance.

9.5 Avionics Discrete I/O

Two discrete I/O pins are available on the D9 connector.

Output specs:
- Open drain output with Vds = 43 V max.
- Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:
- Input interally pulled to 3.3 V via 10 KΩ after input protection diode.
- Input range -0.5 to 43 V max.
- Vil = -0.5 V to 2.4 V
- Vih = 3.0 V to 43 V

9.6 Triggers

9.6.1 Pre-V6 Firmware

One trigger input and one trigger output are available. Although these signals are single-ended, they are controlled as if they were differential.

Input specs:
- Input interally pulled to 3.3V via 10 kΩ.
- Input range -0.5 to 3.6 V max
- Vil = -0.5 V to 0.8 V
- Vih = 1.8 V to 4.1 V
- Zin = 10 KΩ

Output specs:

Voh_max = 3.6 V
Voh_min = 2.4 V min
Vol = 0.45 V max @ 4 ma
Iol / Ioh = 4 mA max
Zout = No output series resistance.

9.6.2 V6 Firmware

Any Avionics discrete and the TRIG_IN can be programmed as a trigger input on a per-channel basis. Any Avionics discrete or TRIG_OUT can be programmed as a trigger output on a per-channel basis.

NOTES

Although TRIG_IN and TRIG_OUT are single-ended, they are controlled as if they were differential via the Trigger Input and Output Control Registers using channel 1. TRIG_OUT can also be controlled using the RS485 Xmit & Control and RS485 Data Global Control Registers for diff 1.

9.7 R15-EC Memory Map Info

The board requires an 8-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

10 • RPCIE-1553 Installation

10.1 RPCIE-1553 Installation Procedure

10.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Remove the cover from the PC. Remove the mounting plate from one of the unused PCIe slots in the computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with the board.

The RPCIE-1553 I/O configuration is defined below. A transition cable is provided from the RPCIE-1553 I/O connector to MIL-STD-1553 cable jacks and a D50 connector for other I/O signals.

10.2 RPCIE-1553 Board Layout

Figure 10-1 RPCIE-1553

10.3 Status LEDs

There are eight LEDs on the mounting plate of the RPCIE-1553:

- **CH 1, CH 2, CH 3, CH 4 – 1553 Bus Activity -** The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic.
- **INIT DONE – Configuration Status** – INIT DONE illuminates green on successful FPGA configuration; The RPCIE-1553 configures from an onboard configuration device, so the INIT DONE LED should be illuminated under normal conditions.
- **PCIE – PCI-Express Link Active** – This LED blinks when the PCI-Express link is active.
- **BIT PASS, BIT FAIL** – **Built-in-test Status –** These LEDs can be controlled by the Application or user. BIT PASS illuminates on successful BIT; BIT FAIL illuminates on failed BIT. Both LEDs are off before the first BIT attempt.

10.4 RPCIE-1553 Connector Description

10.4.1 RPCIE-1553 Front Panel I/O Connector

The RPCIE-1553 uses a single 68-pin SCSI connector (P1) on the mounting plate for all I/O. The mounting plate connector pinout is specified in the following table.

Table 10-1 RPCIE-1553 Front Panel Connector (J1) Pin Assignments

Pin	Function	Pin	Function
1	1553 CH1A+	35	ADISC7/Trigger_0
2	1553 CH 1A-	36	ADISC8/Trigger_1
3	Chassis (See Note)	37	ADISC9/RTADD2_0
4	GND	38	ADISC10/RTADD2_1
5	1553 CH 1B+	39	
6	1553 CH 1B-	40	
7	Chassis (See NOTE)	41	GND
8	RTADDR1_0/ADISC1	42	Trigger_Input+
9	RTADDR1_1/ADISC2	43	Trigger_Input-
10	1553 CH 2A+	44	ADISC11/RTADD2_2
11	1553 CH 2A-	45	ADISC12/RTADD2_3
12	Chassis (See Note)	46	GND
13	GND	47	GND
14	1553 CH 2B+	48	
15	1553 CH 2B-	49	
16	Chassis (See NOTE)	50	GND
17	RTADDR1_2/ADISC3	51	IRIGB IN
18	RTADDR1_3/ADISC4	52	IRIGB OUT
19	1553 CH 3A+	53	IRIGB IN Return

Pin	Function
20	1553 CH 3A-
21	Chassis (See Note)
22	GND
23	1553 CH 3B+
24	1553 CH 3B-
25	Chassis (See Note)
26	~HWRT_EN
27	GND
28	1553 CH 4A+
29	1553 CH 4A-
30	Chassis (See Note)
31	GND
32	1553 CH 4B+
33	1553 CH 4B-
34	Chassis (See Note)

Pin	Function
54	GND
55	ADISC13/RTADD2_4
56	ADISC14/RTADD2_P
57	ADISC15
58	ADISC16
59	
60	
61	GND
62	ADISC17
63	ADISC18
64	RTADDR1_4/ADISC5
65	RTADDR1_P/ADISC6
66	
67	
68	GND

NOTE

These chassis connections are tied to the PCI bracket and may be connected to the MIL-STD-1553 shields, if appropriate.

10.4.2 RPCIE-1553 Transition Cable

Separate Transition Cable assemblies are provided with one-, two- and four-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONQPMC-X section..

10.5 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V
Voh_min = 2.2 V min
Vol = 0.4 V max @ 12 ma
Iol / Ioh = 12 mA max
Zout = No output series resistance.

10.6 Avionics Discrete I/O

Eighteen discrete I/O signals available, twelve of which can be optionally shared with the first two channel's Hardwire RT functionality.

Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:

Input interally pulled to 3.3 V via 4.99 KΩ after input protection diode.
Input range -0.5 to 23 V max.
Vil = -0.5 V to 1.81 V
Vih = 2.18 V to 43 V

10.7 Hardwired RT Address

The RPCIE-1553 provides Hardwired RT Addressing on the first two channels.

10.8 Triggers

10.8.1 Pre-V6 Firmware

One differential trigger input is available.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 500 uA max @ Vin = 12 V, -400 uA max @ Vin = -7 V
Iin = 1000 uA max @ Vin = 25 V, -800 uA max @ Vin = -20 V
Rin = 24 KΩ min.

10.8.2 V6 Firmware

Any Avionics discrete or differential TRIGGER_INPUT can be programmed as a trigger input on a per-channel basis. Any Avionics discrete can be programmed as a trigger output on a per-channel basis.

10.9 Memory Map Info

The board maps into an 8-MByte address block (BAR0). The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

11 • R15-LPCIE Installation

11.1 R15-LPCIE Installation Procedure

11.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Remove the cover from the PC. Remove the mounting plate from one of the unused PCIe slots in the computer. Install the board and bolt the guide plate to the PC with the screw that was removed earlier.

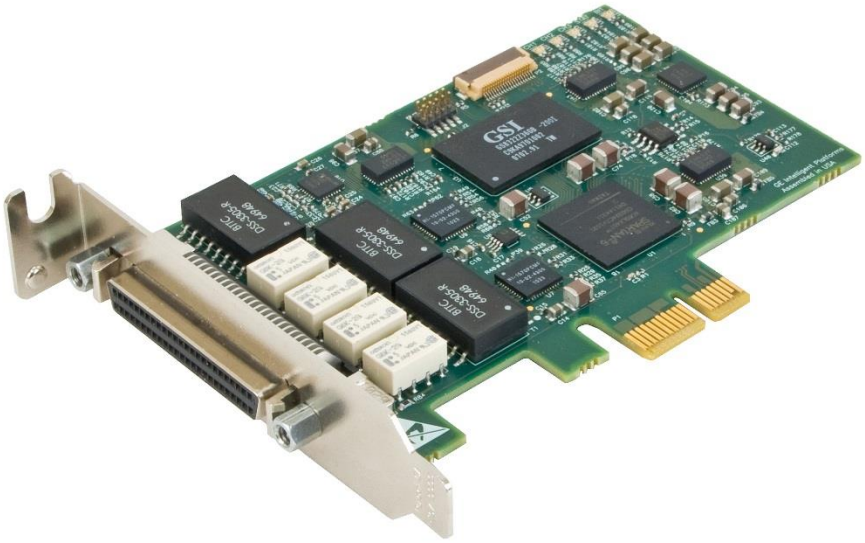
NOTE

The R15-LPCIE is available with two different front panel bezels. One is for standard height applications, and the other is for low profile applications such as servers. Ensure the right bezel is being used for the application.

3. Connect a transition cable assembly to the board to make the required MIL-STD-1553 bus and various I/O connections.

11.2 R15-LPCIE Board Layout

Figure 11-1 R15-LPCIE



11.3 Status LEDs

There are four bi-colored LEDs on the R15-LPCIE:

- **CH 1, CH 2 – 1553 Bus Activity -** The status LED for each 1553 channel illuminates green when receiving 1553 bus traffic, orange when traffic detected, transmit disabled.
- **Status** – This LED illuminates green on successful FPGA configuration from an onboard configuration device and flashes under normal conditions when the PCIe link is active
- **BIT**– **Built-in-test Status –** This LED can be controlled by the Application or user. When used by the firmware, green indicates BIT PASS and red indicates BIT FAIL. The LED is off before the first BIT attempt.

11.4 R15-LPCIE Connector Description

11.4.1 R15-LPCIE Front Panel I/O Connector

The R15-LPCIE uses a single 50-pin SCSI connector (P1) on the mounting plate for all I/O. The bezel connector pinout is specified in the following table.

Table 11-1 R15-LPCIE Front Panel (J1) Pin Assignments

Pin	Function	Pin	Function
1	1553_CH1A-	26	1553_CH1A+
2	Trig_In_CH1	27	Trig_In_CH2
3	GND	28	GND
4	Chassis*	29	IRIG_Out
5	IRIG_Return	30	IRIG_IN
6	ADISC12	31	ADISC 11
7	1553_CH1B-	32	1553_CH1B+
8	ADISC 10	33	ADISC 9
9	ADISC 8	34	ADISC 7
10	GND	35	GND
11	ADISC 6	36	ADISC 5
12	ADISC 4	37	ADISC 3
13	1553_CH2A-	38	1553_CH2A+
14	GND	39	ADISC 2
15	RTAD0	40	ADISC 1
16	Chassis*	41	GND
17	RTAD3	42	RTAD1
18	RTAD4	43	RTAD2
19	1553_CH2B-	44	1553_CH2B+
20	RTADP	45	Trig_Out_CH1
21	485_NEG1	46	485_POS1

Pin	Function
22	485_NEG2
23	Reserved
24	Chassis*
25	Reserved

Pin	Function
47	485_POS2
48	Reserved
49	Trig_Out_CH2
50	Reserved

NOTE

The Chassis connections are tied to the LPCIe bracket and are intended to be used as the MIL-STD-1553 shields.

11.4.2 R15-LPCIE Transition Cable

A mating connector is provided with the card and Transition Cable assemblies are available for one and two-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONR15-LPCIE-X section.

11.5 IRIG Signaling

IRIG input and output signals are provided. Software-selectable internal wrap.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.47 V - Zout drop
Voh_min = 2.75 V min - Zout drop
Vol = 0.4 V max + Zout drop
Iol / Ioh = 12 mA max
Zout = 49.9 Ω output series resistance.

11.6 Avionics Discrete I/O

The R15-LPCIE has twelve discrete I/O signals (ADISC X) available on the interface connector. Outputs have short circuit protection with auto restart.

Output specs:
Open drain output with Vds = 60 V max.
Vol = 0.35 V max @ Iol = 500 mA.

Input specs:
Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 60 V max
Vil = -0.5 V to 1.8 V
Vih = 2.2 V to 60 V.

11.7 External RT Address

The R15-LPCIE provides Hardwired RT Addressing through dedicated (RTADX) pins. Flash based RT addressing is also available.

Input specs:

Input range -0.3 to 5.5 V max.
Input pulled to 5V via 866Ω

11.8 Differential I/O

Two differential I/O (485_X) with software-switchable 120-Ω termination resistors provided. They can be used single-ended as well since the negative terminal is biased at ~ 1.8V.

Output specs:

Vod (differential) = 2 V min into 50 Ω load, 3.3 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 125 uA max @ Vin = 12 V, -100 uA max @ Vin = -7 V
Rin = 96 KΩ min not taking into account Vneg_bias resistors.

Negative pin bias:

Vneg_bias = ~1.8 V via 10 KΩ pull-up to 3.3V and 13 KΩ pull-down to ground.

11.9 Triggers

Each 1553 channel includes a dedicated input (TRIG_IN_CHX) and output trigger (TRIG_OUT_CHX).

Output specs:

Voh_max = 3.47 V - Zout drop
Voh_min @ Ioh = -100 uA = 2.9 V - Zout drop
Voh_min @ Ioh = -16 mA = 2.4 V - Zout drop
Vol_max @ Iol = -100 uA = 0.1 V + Zout drop
Vol_max @ Iol = -16 mA = 0.4 V + Zout drop
Iol / Ioh = 24 mA max
Zout = 100 Ω output series resistance.

Input specs:

Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 60 V max.
Vil = -0.5 V to 1.5 V
Vih = 2.0 V to 60 V

12 • RXMC-1553 Installation

NOTE

If you purchased the RXMC-1553-TB variant of this product, please also refer to the "TB3-TO-CMC-LP Thunderbolt™ 3 Expansion Adapter User's Guide" provided with the product or also available on the Abaco website (https://www.abaco.com/TB3LP_Guide). This document contains important additional information for operating in a Thunderbolt environment.

12.1 Installation Procedure

This section tells how to install the RXMC-1553 board. The RXMC-1553 is a XMC.3 product with one or two 1553 channels.

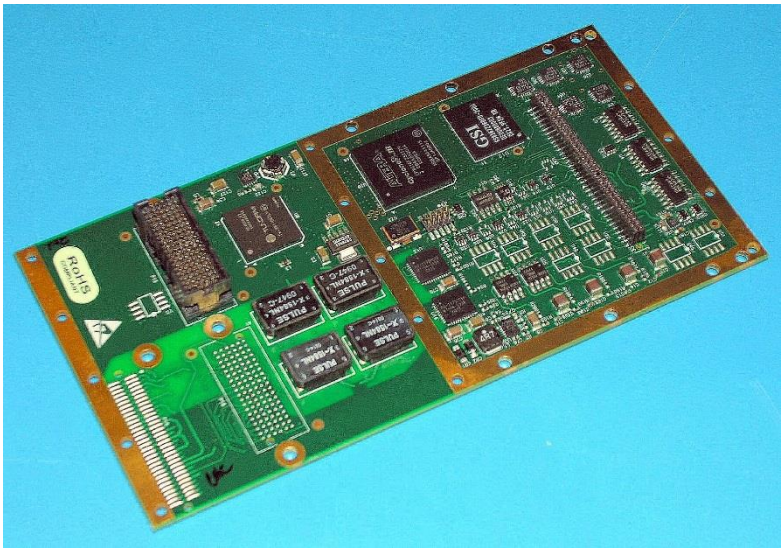
12.1.1 Hardware Installation

After installing the software, follow the steps below to install the hardware. The RXMC-1553 installs in XMC.3 [PCI Express only] sites.

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Insert the RXMC-1553 into the XMC site.
3. I/O for the RXMC is present on P14, P16 or front I/O as a factory configuration option.

12.2 RXMC-1553

Figure 12-1 RXMC-1553



12.3 RXMC-1553 Connector Description

The RXMC-1553 implements the PCI Express interface on P15. The RXMC-1553 uses either P14 or P16 for rear I/O, with front panel I/O available as a factory option.

12.3.1 RXMC-1553 P16 Pin Assignments

Table 12-1 P16 Connector Mapping Assignment RXMC-1553, All I/O Options Installed

Pin	Function	Pin	Function
B5* C2	CH1 A-	A5* C1	CH1 A+
B7* C4	CH1 B-	A7* C3	CH1 B+
C7	IRIG out	All Even Pins, Rows A, B, D, E	GND
E5	CH2 A-	D5	CH2 A+
E7	CH2 B-	D7	CH2 B+
C11	CH1 RTAD1	C10	CH1 RTAD0
C13	CH1 RTAD3	C12	CH1 RTAD2
C15	CH1 RTADPTY	C14	CH1 RTAD4
F1	SHIELD (Chassis)	F2	SHIELD (Chassis)
F8	CH1 EXTTRIG	F9	CH2 EXTTRIG
F12	PIO0 / EIA0N / DISC5	F16	PIO4 / EIA2N / DISC9
F13	PIO1 / EIA0P / DISC6	F17	PIO5 / EIA2P / DISC10
F14	PIO2 / EIA1N / DISC7	F18	PIO6 / EIA3N / DISC11
F15	PIO3 / EIA1P / DISC8	F19	PIO7 / EIA3P / DISC12
C8	IRIG In	C9	IRIG Return
F4	RTN_Discrete 1	C16	28V_Discrete 1
F5	RTN_Discrete 2	C17	28V_Discrete 2
F6	RTN_Discrete 3	C18	28V_Discrete 3
F7	RTN_Discrete 4	C19	28V_Discrete 4

NOTE

* Indicates Preferred Pin

12.3.2 RXMC-1553 P14 Pin Assignments

Table 12-2 P14 Connector Mapping Assignment RXMC-1553, All I/O Options Installed

Pin	Function	Pin	Function
1	CH1 A-	2	CH1 A+
3	Shield (Chassis)	4	Shield (Chassis)
5	CH1 A-	6	CH1_A+
7	CH1 B-	8	CH1 B+
9	Shield (Chassis)	10	Shield (Chassis)
11	CH1 B-	12	CH1 B+
13	GND	14	GND
15	CH2 A-	16	CH2 A+
17	Shield (Chassis)	18	Shield (Chassis)
19	CH2 A-	20	CH2 A+
21	CH2 B-	22	CH2 B+
23	Shield (Chassis)	24	Shield (Chassis)
25	CH2 B-	26	CH2 B+
27	GND	28	GND
29	CH1 RTAD1	30	CH1 RTAD0
31	CH1 RTAD3	32	CH1 RTAD2
33	CH1 RTADPTY	34	CH1 RTAD4
35	GND	36	GND
37	CH1 EXTTRIG	38	CH2 EXTTRIG
39	*no connection*	40	*no connection*
41	GND	42	*no connection*
43	*no connection*	44	*no connection*
45	*no connection*	46	IRIG_OUT
47	PIO0 / EIA0N / DISC5	48	PIO4 / EIA2N / DISC9
49	PIO1 / EIA0P / DISC6	50	PIO5 / EIA2P / DISC10
51	PIO2 / EIA1N / DISC7	52	PIO6 / EIA3N / DISC11
53	PIO3 / EIA1P / DISC8	54	PIO7 / EIA3P / DISC12
55	IRIG_IN	56	IRIG_RTN
57	RTN_DISC1	58	28V_DISC1
59	RTN_DISC2	60	28V_DISC2
61	RTN_DISC3	62	28V_DISC3
63	RTN_DISC4	64	28V_DISC4

12.3.3 RXMC-1553 Front Panel Pin Assignments

Table 12-3 RXMC-1553 Connector Pin Assignments Front Bezel Connector

Pin	Function	Pin	Function
1	CH1 A+	35	CH1 EXTTRIG
2	CH1 A-	36	CH2 EXTTRIG
3	Shield (Chassis)	37	*no connection*
4	GND	38	*no connection*
5	CH1 B+	39	PIO0 / EIA0N / DISC5
6	CH1 B-	40	PIO1 / EIA0P / DISC6
7	Shield (Chassis)	41	RTN_DISC1
8	CH1 RTAD0	42	RTN_DISC2
9	CH1 RTAD1	43	RTN_DISC3
10	CH2 A+	44	*no connection*
11	CH2 A-	45	*no connection*
12	Shield (Chassis)	46	RTN_DISC4
13	GND	47	GND
14	CH2 B+	48	PIO2 / EIA1N / DISC7
15	CH2 B-	49	PIO3 / EIA1P / DISC8
16	Shield (Chassis)	50	GND
17	CH1 RTAD2	51	IRIGB IN
18	CH1 RTAD3	52	IRIGB OUT
19	*no connection*	53	IRIGB RTN
20	*no connection*	54	GND
21	*no connection*	55	*no connection*
22	GND	56	*no connection*
23	*no connection*	57	28V_DISC1
24	*no connection*	58	28V_DISC2
25	*no connection*	59	PIO4 / EIA2N / DISC9
26	*no connection*	60	PIO5 / EIA2P / DISC10
27	GND	61	GND
28	*no connection*	62	28V_DISC3
29	*no connection*	63	28V_DISC4
30	*no connection*	64	CH1 RTAD 4
31	GND	65	CH1 RTADPTY
32	*no connection*	66	PIO6 / EIA3N / DISC11

Pin	Function
33	*no connection*
34	*no connection*

Pin	Function
67	PIO7 / EIA3P / DISC12
68	GND

* Indicates Preferred Pin

12.3.4 RXMC-1553 Signal Descriptions

Table 12-4 Signal Descriptions

Mnemonic	Description
CH1 A+	MIL-STD-1553 Channel 0, Bus A positive differential half
CH1 A-	MIL-STD-1553 Channel 0, Bus A negative differential half
CH1 B+	MIL-STD-1553 Channel 0, Bus B positive differential half
CH1 B-	MIL-STD-1553 Channel 0, Bus B negative differential half
CH2 A+	MIL-STD-1553 Channel 1, Bus A positive differential half
CH2 A-	MIL-STD-1553 Channel 1, Bus A negative differential half
CH2 B+	MIL-STD-1553 Channel 1, Bus B positive differential half
CH2 B-	MIL-STD-1553 Channel 1, Bus B negative differential half
Shield (chassis)	Can be used to terminate the incoming 1553 cabling shield, on rear I/O cards this is connected to the host card thermal frame (unconnected if thermal frame not present on host card). On front I/O cards signal this may be connected to the bezel through the addition of four zero ohm 0402 resistors (R270, R273, R274, R275).
CH1RTAD0 to CH1RTAD4	Channel 1 RT Address bits 0 to 4. Used to set the address of an RT. Only valid in RT mode. Connect to ground for a logic “0” or leave open for a logic “1”. To enable software RT address selection, leave these signals open. Channel 2’s RT address is indexed relative to the value present here (refer to Universal Core Architecture Manual for further information on address indexing).
CH1RTADPTY	Channel 1 RT Address Parity. Only valid in RT mode. It must provide the odd parity sum with CH1RTAD0 to CH1RTAD4. Connect to ground for a logic “0” or leave open for a logic “1”. To enable software RT address selection, leave this signal open
CH1EXTTRIG	Channel 0 External Trigger/flag. A multi-functional input depending on the mode of operation. In RT mode, setting this line low sets the Subsystem Flag bit in the RT Status Word. In BC mode, if the external trigger has been enabled through software, a low-to-high transition on this line starts execution of the current BC frame
CH2EXTTRIG	As above, but for Channel 1
DISC[12:5]	Bidirectional avionic discretes
28V_DISC[4:1]	For open / ground discretes: this pin is the connection for the external high side load.
	For 28V/open discretes: Power source (8-43V) for the switched low side load.
RTN_DISC[4:1]	For open / ground discretes: Return for switched high side load. User to connect to GND.
	For 28V/open discretes: the connection for the external low side load.
PIO[7:0]	8-bit TTL-compatible parallel I/O port

Mnemonic	Description
EIA[3:0]P, EIA[3:0]N	EIA-485 differential discrete I/O
IRIG_IN	IRIGB input (positive for differential signal), DC Level Shifted or Amplitude Modulated
IRIG_RTN	IRIGB input, return or inverted signal for differential signaling
IRIG_OUT	TTL compatible output of IRIG generator, DC level shifted only

12.3.5 RXMC-1553 Transition Cables

Separate Transition Cable assemblies are provided with one or two-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONQPMC-X section.

12.3.6 I/O Options

The RXMC-1553 is available with a variety of I/O options. However, I/O connector pins are limited. Thus, individual connector pins can have a different I/O function based on the purchased configuration of the card.

12.4 Trigger Inputs

Each 1553 channel has a dedicated Trigger Input signal.

Input specs:

Input interally pulled to 3.3V via 49.9 KΩ series resistor and protection diode.
Input range -0.5 to 4.5 V max
Vil = -0.5 V to 0.8 V
Vih = 1.7 V to 4.5 V.

12.5 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.6 V min - Zout drop
Vol = 0.4 V max + Zout drop
Iol / Ioh = 12 mA max
Zout = 49.9 Ω output series resistance.

12.6 Avionics Discrete I/O

A maximum of twelve Avionics Discretes are available but there may be less due to the purchased configuration.

Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.2 V max @ Iol = 0.5 A

Input specs:

Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 43 V max
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V.

12.7 Differential Discrete I/O

A maximum of four Differential I/O are available but there may be less due to the purchased configuration. A 121 Ω termination is an option.

Output specs:

Vod (differential) = 1.5 V min into 54 Ω load, 3.6 V max.
Voc (common mode) = 2.5 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 110 uA max @ Vin = 12 V, -100 uA min @ Vin = -7 V
Rin = 24 KΩ min not taking into account Vneg_bias resistors.

12.8 Hardwired RT Address

The RXMC-1553 provides dedicated Hardwired RT Addressing on channel 0. Flash based RT addressing is also available.

Input specs:

Input range -0.3 to 5.5 V max.
Input pulled to 5V via 866Ω

12.9 Parallel I/O (PIO)

The Parallel I/O or PIO are a bank of 8-eight TTL-level signals which may be available depending on the purchased configuration. These signals are provided by a device which is serially controlled and as such, can take around 25 µs to react from the time of the issuing command.

Output specs:

Voh = 2.3 V min to 3.6 V max.
Vol = 0.6 V max @ Iol = 3 ma.

Input specs:

Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 43 V max
Vil = -0.5 V to 0.6 V
Vih = 2.9 V to 3.6 V

12.10 28 V Discrete I/O

A maximum of four 28 V Discretes are available but there may be less due to the purchased configuration.

As 28 V Driver:

Power source to 28V_DISCx can be 8-43V
RTN_DISCx will provide switched 8-43V
Vdrop ~ 0.1 V @ Iol max = -0.5 A,

As 28 V Ground:
Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 0.5 A

12.11 RXMC-1553 Memory Map Info

The board requires an 8-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

13 • RXMC2-1553 Installation

13.1 Installation Procedure

This section tells how to install the RXMC2-1553 board. The RXMC2-1553 is an XMC.3 product with one, two or four 1553 channels.

13.1.1 Hardware Installation

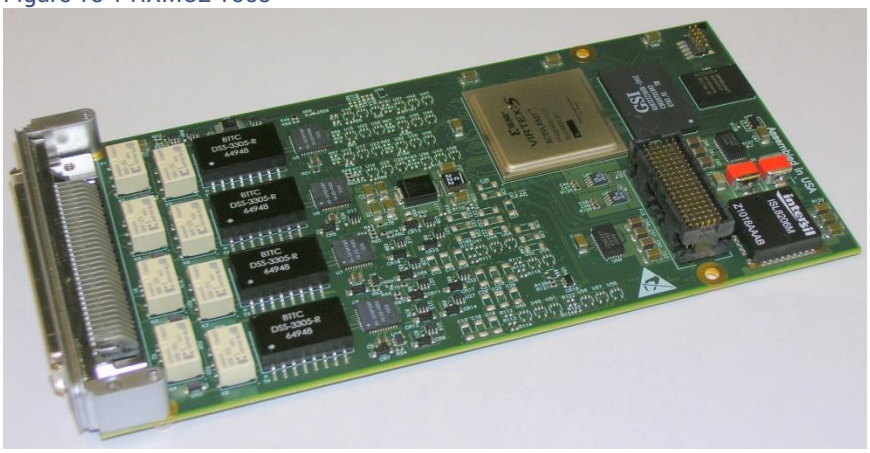
After installing the software, follow the steps below to install the hardware. The RXMC2-1553 installs in XMC.3 [PCI Express only] sites.

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Insert the RXMC2-1553 into the XMC site.

I/O for the RXMC2 is present on front bezel connector.

13.2 RXMC2-1553

Figure 13-1 RXMC2-1553



13.3 RXMC2-1553 Connector Description

The RXMC2-1553 implements the PCI Express interface on P15 and uses front panel I/O for all other signals.

13.3.1 RXMC2-1553 Front Panel I/O Connector

The RXMC2-1553 includes a thru-bezel I/O connector. A mating connector is included with the RXMC2-1553. Pin assignments are described in the following table:

Table 13-1 RXMC2-1553 Connector Pin Assignments Front I/O Connector

Pin	Function	Pin	Function
1	1553_CH4B+	35	1553_CH4B-
2	1553_CH4A+	36	1553_CH4A-
3	DISCRETE1	37	DISCRETE2
4	DISCRETE3	38	DISCRETE4
5	DISCRETE5	39	DISCRETE6
6	GND	40	GND
7	DISCRETE7	41	DISCRETE8
8	DISCRETE9	42	DISCRETE10
9	DISCRETE11	43	DISCRETE12
10	GND	44	GND
11	1553_CH3B+	45	1553_CH3B-
12	1553_CH3A+	46	1553_CH3A-
13	Reserved	47	Reserved
14	TRIG_IN_CH1	48	TRIG_IN_CH2
15	TRIG_IN_CH3	49	TRIG_IN_CH4
16	Reserved	50	Reserved
17	Reserved	51	Reserved
18	Reserved	52	Reserved
19	Reserved	53	Reserved
20	Reserved	54	Reserved
21	Reserved	55	Reserved
22	Reserved	56	Reserved
23	Reserved	57	Reserved
24	Reserved	58	Reserved
25	1553_CH2B+	59	1553_CH2B-
26	1553_CH2A+	60	1553_CH2A-
27	Reserved	61	Reserved
28	Reserved	62	Reserved
29	EXT_TT_CLK_A	63	EXT_TT_CLK_B
30	EXT_TT_RST_A	64	EXT_TT_ RST_B

Pin	Function
31	GND
32	IRIG_IN+
33	1553_CH1B+
34	1553_CH1A+

Pin	Function
65	IRIG_TX
66	IRIG_IN-
67	1553_CH1B-
68	1553_CH1A-

13.3.2 RXMC2-1553 Transition Cable

Transition Cable assemblies are available for two and four-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONRXMC2-X section.

13.4 Trigger Inputs

Each 1553 channel has a dedicated Trigger Input signal.

Input specs:
Vil = -0.2 V to 0.8 V
Vih = 2.0 V to 3.45 V
Zin = 10 KΩ input series resistance.

13.5 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V
Voh_min = 2.2 V min
Vol = 0.4 V max @ 12 ma
Iol / Ioh = 12 mA max
Zout = No output series resistance.

13.6 Avionics Discrete I/O

Twelve Avionics Discrete signals are provided.

Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.35 V max @ Iol = 500 mA.

Input specs:

Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 43 V max
Vil = -0.5 V to 2.0 V
Vih = 2.4 V to 43 V.

13.7 Differential I/O

A differential clock input and a differential time-tag reset input are provided. The differential clock input accepts a 1-MHz external clock in under software control, and the reset input resets the card's time-tag to zero upon receipt of a valid input signal. Software can enable/disable the 121 Ω termination.

Output specs:

Vod (differential) = 2 V min into 50 Ω load, 3.3 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = $\pm$0.2 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 125 uA max @ Vin = 12 V, -100 uA max @ Vin = -7 V
Rin = 96 KΩ min.

13.8 Hardwired RT Address

The RXMC2-1553 provides RT Addressing only through non-volatile storage in Flash memory.

13.9 RXMC2-1553 Memory Map Info

The board requires an 8-Mbyte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

14 • QVME-1553, RQVME2-1553 and QVXI2-1553X Installation

14.1 Installation Procedure

This section tells how to install the QVME / RQVME2 / QVXI2 hardware and software.

NOTE

The QVME-1553 has been discontinued.

NOTE

RQVME2-1553 is a RoHS direct replacement for the QVME-1553 with no functional difference. Throughout this document, "QVME-1553" also refers to both QVXI-1553X and RQVME2-1553 products unless otherwise stated.

14.1.1 Hardware Installation

Follow these steps to install the hardware:

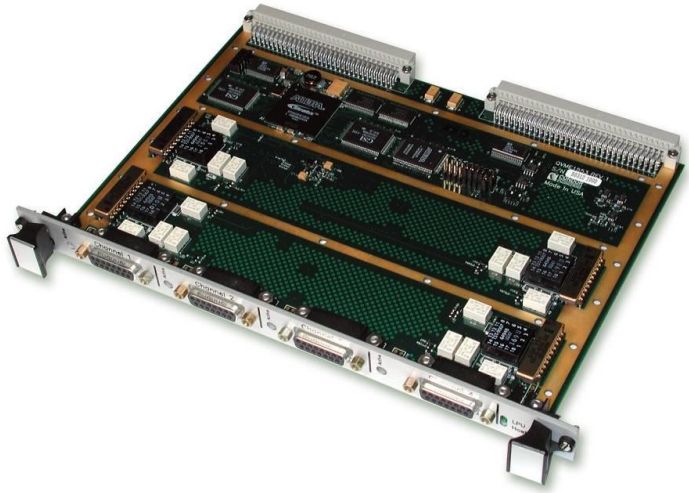
1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Install the board into the VME chassis. Take into account the other VME boards in the chassis and chassis design when installing the board.
3. Connect the transition cable assembly to the board and then connect the MIL-STD-1553 bus to the cable assembly provided with the board.

14.2 RQVME2-1553

Figure 14-1 RQVME2-1553

14.3 QVME-1553

Figure 14-2 QVME-1553



14.4 QVXI2-1553X

Figure 14-3 QVXI2-1553X

14.5 QVME / QVXI2 Connector Descriptions

14.5.1 QVME / QVXI2 Front Panel Pinouts

The QVME and QVXI2 1553 products provide four DB15 front panel connectors, P3 through P6 which corresponds to 1553 channels 1 through 4 respectively. These boards have one-, two- and four-channel configurations available. Table 14-1 shows the pin assignments.

Table 14-1 QVME / QVXI2 -1553 Front Panel Pin Assignments

Front Panel Connector P(3,4,5,6) for Channel(1,2,3,4) Interface			
Pin	Signal	Pin	Signal
1	BUSn_B+	9	BUSn_SHIELD
2	BUSn_B-	10	No connection
3	GND	11	GND*
4	BUSn_A+	12	IRIGB_IN*
5	BUSn_A-	13	IRIGB_IN Return*
6	BUSn_SHIELD	14	GND*
7	BUSn_TRIGIN	15	IRIGB_OUT*
8	BUSn_TRIGOUT		

NOTE

* These signals available on QVME-1553 and QVXI2-1553X ONLY, No connection on RQVME2-1553.

14.5.2 QVME / QVXI2-1553 Transition Cables

Depending on the boards 1553 channel count and IRIG availability, each board is supplied with one, two or four transition cables which mate with the DB15 connector(s).

Cable information and pinouts for the transition cables are provided in the Appendix A RCONP1553-1 section for non-IRIG boards and CONW1553-1 section for IRIG boards.

14.5.3 RQVME2-1553 P2 Connector

Table 14-2 RQVME2-1553 P2 Connector Pinout

Pin	Row A	Row B	Row C
1	CH0_RTA0/CH0_DC_A+	+5 VDC	CH2_RTA0/CH2_DC_A+
2	CH0_RTA1/CH0_DC_A-	GND	CH2_RTA1/CH2_DC_A-
3	CH0_RTA2/CH0_DC_B+	N/C	CH2_RTA2/CH2_DC_B+
4	CH0_RTA3/CH0_DC_B-	A24	CH2_RTA3/CH2_DC_B-
5	CH0_RTA4	A25	CH2_RTA4
6	CH0_RTAP	A26	CH2_RTADP
7	CH0_SHIELD	A27	CH2_SHIELD
8	CH0_A+	A28	CH2_A+
9	CH0_A-	A29	CH2_A-
10	CH0_B+	A30	CH2_B+
11	CH0_B-	A31	CH2_B-
12	CH0_TRIG_IN	GND	CH2_TRIG_IN
13	CH0_TRIG_OUT	+5 VDC	CH2_TRIG_OUT
14	CH1_A+	D16	CH3_A+
15	CH1_A-	D17	CH3_A-
16	CH1_B+	D18	CH3_B+
17	CH1_B-	D19	CH3_B-
18	CH1_SHIELD	D20	CH3_SHIELD
19	GND	D21	CH3_RTA0
20	IRIGB_IN	D22	CH3_RTA1RTA1
21	IRIGB_IN Return	D23	CH3_RTA2H3_RTA2
22	CH1_RTA0/CH1_DC_A+	GND	CH3_RTA3/CH3_DC_A+
23	CH1_RTA1/CH1_DC_A-	D24	CH3_RTA4/CH3_DC_A-
24	CH1_RTA2/CH1_DC_B+	D25	CH3_RTADP/CH3_DC_B+
25	CH1_RTA3/CH1_DC_B-	D26	CH3_TRIG_IN/CH3_DC_B-
26	CH1_RTA4	D27	CH3_TRIG_OUT

Pin	Row A	Row B	Row C
27	CH1_RTADP	D28	DISCRETE_1
28	CH1_TRIG_IN	D29	DISCRETE_2
29	CH1_TRIG_OUT	D30	GND
30	MODID	D31	DISCRETE_3
31	IRIGB_OUT	GND	DISCRETE_4
32	CH0_TX	+5 VDC	GND

14.5.4 QVXI-1553X P2 Connector

Table 14-3 QVXI-1553X P2 Connector Pinout

Pin	Row A	Row B	Row C
1	N/A	+5 VDC	N/A
2	N/A	GND	N/A
3	N/A	N/C	N/A
4	N/A	A24	N/A
5	N/A	A25	N/A
6	N/A	A26	N/A
7	N/A	A27	N/A
8	N/A	A28	N/A
9	N/A	A29	N/A
10	N/A	A30	N/A
11	N/A	A31	N/A
12	N/A	GND	N/A
13	N/A	+5 VDC	N/A
14	N/A	D16	N/A
15	N/A	D17	N/A
16	N/A	D18	N/A
17	N/A	D19	N/A
18	N/A	D20	N/A
19	N/A	D21	N/A
20	N/A	D22	N/A
21	N/A	D23	N/A
22	N/A	GND	N/A
23	N/A	D24	N/A
24	N/A	D25	N/A
25	N/A	D26	N/A

Pin	Row A	Row B	Row C
26	N/A	D27	N/A
27	N/A	D28	N/A
28	N/A	D29	N/A
29	N/A	D30	N/A
30	MODID	D31	N/A
31	N/A	GND	N/A
32	N/A	+5 VDC	N/A

14.5.5 QVME-1553 P2 Connector

Table 14-4 QVME-1553 P2 Connector Pinout

Pin	Row A	Row B	Row C
1	CH0_RTA0	+5 VDC	CH2_RTA0
2	CH0_RTA1	GND	CH2_RTA1
3	CH0_RTA2	N/C	CH2_RTA2
4	CH0_RTA3	A24	CH2_RTA3
5	CH0_RTA4	A25	CH2_RTA4
6	CH0_RTADP	A26	CH2_RTADP
7	CH0_SHIELD	A27	CH2_SHIELD
8	CH0 A+	A28	CH2 A+
9	CH0 A-	A29	CH2 A-
10	CH0 B+	A30	CH2 B+
11	CH0 B-	A31	CH2 B-
12	CH0_TRIG_IN	GND	CH2_TRIG_IN
13	CH0_TRIG_OUT	+5 VDC	CH2_TRIG_OUT
14	CH1 A+	D16	CH3 A+
15	CH1 A-	D17	CH3 A-
16	CH1 B+	D18	CH3 B+
17	CH1 B-	D19	CH3 B-
18	CH1_SHIELD	D20	CH3_SHIELD
19	GND	D21	CH3_RTA0
20	IRIGB_IN	D22	CH3_RTA1RTA1
21	IRIGB_IN Return	D23	CH3_RTA2H3_RTA2
22	CH1_RTA0	GND	CH3_RTA3
23	CH1_RTA1	D24	CH3_RTA4

Pin	Row A	Row B	Row C
24	CH1_RTA2	D25	CH3_RTADP
25	CH1_RTA3	D26	CH3_TRIG_IN
26	CH1_RTA4	D27	CH3_TRIG_OUT
27	CH1_RTADP	D28	DISCRETE_1
28	CH1_TRIG_IN	D29	DISCRETE_2
29	CH1_TRIG_OUT	D30	GND
30	MODID	D31	DISCRETE_3
31	IRIGB_OUT	GND	DISCRETE_4
32	CH0_TX	+5 VDC	GND

14.5.6 QVXI2-1553X P2 Connector

Since the QVXI2-1553X consists of a RQVME2-1553 installed on a C-size VME to VXI extender, rear I/O is limited to the 32-bit VME interface specified by the VXI Consortium. No rear I/O is supported in this configuration.

14.5.7 Transformer versus Direct Coupling

MIL-STD-1553B allows for two methods of connecting a terminal to the bus.

- **Transformer coupling** provides noise immunity over long distances and requires external transformer couplers.
- **Direct coupling** is often used in the laboratory because it requires no transformers between boxes.

14.5.8 MIL-STD-1553B Signals

Shields for both A and B busses are tied together and to the center tap of the isolation transformers on the QVME-1553, RQVME2-1553 and QVXI2-1553X boards.

14.6 Trigger Input

A trigger input is provided on all boards.

Input specs:
Input interally pulled to 3.3V via 4.7 kΩ.
Input range -0.5 to 4.1 V max
Vil = -0.5 V to 0.8 V
Vih = 1.8 V to 4.1 V

14.7 Trigger Output

A trigger output is provided on all boards.

Output specs:
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop
Iol / Ioh = 12 mA max
Zout = 330 Ω output series resistance.

14.8 Discrete I/O

The QVME-1553 has four discrete I/O pins available on the VME P2 connector. The QVXI2-1553X also has four discrete I/O pins available on the VME P2 connector. Routing these to the backplane through the jumper connector provided with the VXI extender is not recommended. However, these signals may be brought to the front panel through an adapter available from the extender manufacturer.

Output specs:
Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:
Input interally pulled to 3.3 V via 22 KΩ after input protection diode.
Input range -0.5 to 43 V max.
Vil = -0.5 V to 2.5 V
Vih = 2.8 V to 43 V

14.9 Hardwired RT Address

The QVME-1553 provides Hardwired RT Addressing on all channels. This operational mode is enabled by installing a shunt across JB1:17-18.

Hardwired RT Addressing is not available on QVXI2-1553X, as the rear I/O connector is designated for VXI signals ONLY. Contact Abaco Sales for special requirements.

Input specs:
Input range -0.5 to 4.1 V max
Vil = -0.5 V to 0.8 V
Vih = 1.8 V to 4.1 V
Zin = unknown but very high

14.10 IRIG Signaling

The QVME-1553 have optional IRIG-B capability.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

14.11 Memory Map Info

The QVME-1553 uses A16 addressing for the configuration register and either A24 or A32 for addressing the 1553 channels. The base address of the A16 configuration register is (ID * 0x40) + 0xC000. Set ID using the eight VXI jumpers (VXI A0 – VXI A7) on JB1. These jumpers are asserted (1) when unconnected and de-asserted (0) when connected. This provides a range of A16 addresses from 0xC000 to FFC0. A 0x40 byte region within this range (and that does not interfere with any other devices) must be specified.

The QVME-1553 uses an 8-Mbyte address block to address up to four separate 1553 channels. This allows both A24 and A32 addressing to access all channels. The base address for the board is programmable and must be supplied during initialization. The base address must have sufficient room to allow mapping of 8-MBytes without interfering with other devices in the system.

The A24/A32 address is programmed by writing the board's base address to the offset register (byte address offset 6) in the A16 configuration space. A24 or A32 addressing is selected by writing to bit 3 of the Control Register (byte address offset 8). Writing a "0" selects A24 addressing, writing a "1" selects A32 address. If A32 addressing is selected, the base address must be on an even 512-Kbyte boundary. If A24 addressing, only 0x0 or 0x800000 may be used as the base address. See the "MIL-STD-1553 Universal Core Architecture Reference Manual" (1600100-0001) for details of the A16 register usage.

The supplied software supports the QVME-1553 under 32-Bit Windows using National Instruments NI-VXI interface and VxWorks.

15 • Q104-1553 and Q104-1553-P Installation

15.1 Installation Procedure

This section explains how to install the Q104-1553 and Q104-1553-P boards. The Q104-1553 is an ISA bus PC/104 form factor board. The Q104-1553-P is a Universal-voltage PCI bus PC/104-*Plus* form factor board.

 NOTE

Both boards have been discontinued.

15.1.1 Hardware Installation

After installing the software, follow the steps to install the hardware:

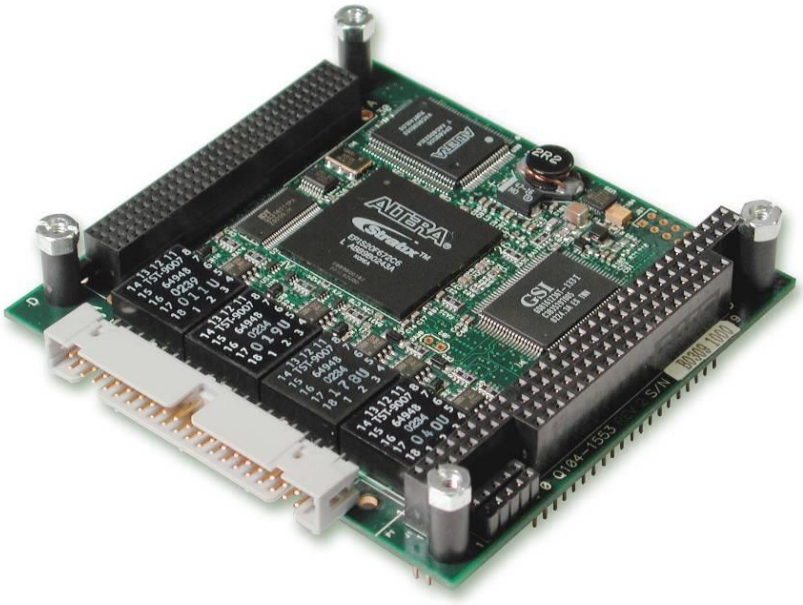
1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the jumpers are changed.
2. The Q104 uses jumpers to select installation location. Boards that are configured for the ISA interface (Q104-1553) use JB1 to select ISA base address. Boards that use the PCI interface (Q104-1553-P) use the jumpers at JB1 to select the PC/104-*Plus* stack location.
3. Set the jumpers on the Q104-1553 board to the desired settings for the operating system.
4. Insert the board into the PC/104 chassis.

 NOTE

Mount hardware is captive to the ISA and PCI connectors (where applicable).

5. A mating connector and retaining clip is provided for the I/O interface.

Figure 15-1 Q104-1553, with Optional PC/104-*Plus* interface



15.2 Q104-1553 and Q104-1553-P Connector Description

The Q104-1553 connectors J1 and J2 implement the 16-bit ISA bus interface. Additionally, on Q104-1553-P configurations, J3 is installed for the PC/104-*Plus* PCI interface.

The board I/O signals are all routed to connector P1. Pin assignments are listed in Table 15-1.

Table 15-1 Q104-1553 / Q104-1553-P P1 Connector Pin Assignments

Pin	Function	Pin	Function
1	1553_CH1 A+	2	1553_CH1 Shield
3	1553_CH1 A-	4	GND
5	1553_CH1 B+	6	RS-485 Shield
7	1553_CH1 B-	8	IRIGB In Return
9	RS-485 0+	10	IRIGB In
11	RS-485 0-	12	IRIGB Out
13	RS-485 1+	14	Discrete I/O 1/ RTADDR1
15	RS-485 1-	16	Discrete I/O 2/ RTADDR2
17	1553_CH2 A+	18	Discrete I/O 3/ RTADDR3
19	1553_CH2 A-	20	Discrete I/O 4/ RTADDR4
21	1553_CH2 Shield	22	Discrete I/O 5/ RTADDR5
23	1553_CH2 B+	24	GND
25	1553_CH2 B-	26	Discrete I/O 6/ RTADDRP
27	1553_CH3 A+	28	Discrete I/O 7

Pin	Function
29	1553_CH3 A-
31	1553_CH3 Shield
33	1553_CH3 B+
35	1553_CH3 B-
37	1553_CH4 A+
39	1553_CH4 A-

Pin	Function
30	Discrete I/O 8
32	Discrete I/O 9
34	Discrete I/O 10
36	1553_CH4 B-
38	1553_CH4 B+
40	1553_CH4 Shield

NOTE

P1 pin assignments flow from pin 1 to pin 40 as would be seen from the perspective of a ribbon cable assembly. Therefore, pins 1 and 2 are top-bottom adjacent on the connector and ribbon, located nearest the PC/104 connector, J1. Pin 1 is indicated by a square pad, visible from solder side of the card.

15.2.1 Q104-1553 and Q104-1553-P Transition Assemblies

The Q104-1553 and Q104-1553-P ship with a connector mate for P1, which may be used to assemble a custom cable to mate to MIL-STD-1553 wiring as well as the other available I/O.

15.3 Setting the MEM16 Decode

Onboard jumpers are assigned to the “usa” bit that forces the hardware to decode the ISA sa[16…14] signals along with the la[23…17] signals as qualifiers for the MEM16 signal. MEM16 is the asynchronous handshake that informs the initiator that it can accept a 16-bit word transfer (PC/AT 16-bit board versus 8-bit XT board). The EISA/ISA specification does not allow sa[] signals to be used to qualify MEM16, as the adapters within a 128-KByte boundary must all be 16-bit or all be 8-bit boards. Many platforms do not follow the specification, and qualifying MEM16 with sa[16…14] works best on the vast majority of ISA platform PCs. However, a very few PCs delay the sa[] signals too long to qualify them for MEM16.

By default, the board uses sa[16…14] to qualify MEM16. Contact Abaco Systems Technical Support to disable usage of the MEM16 signal.

15.4 IRIG Signaling

IRIG input and output signals are provided.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.4 V min - Zout drop

Vol = 0.4 V max + Zout drop @ 16 ma
Iol / Ioh = 12 mA max
Zout = 10 Ω output series resistance.

15.5 Avionics Discrete I/O

Both boards have ten discrete I/O signals, six of which can be optionally shared with the first channel's Hardwire RT functionality.

Output specs:

Open drain output with Vds = 43 V max.
Vol = 0.3 V max @ Iol = 1 A, 0.2 V max @ Iol = 100 mA

Input specs:

Input interally pulled to 5 V via 22 KΩ after input protection diode.
Input range -0.5 to 43 V max.

Q104-1553
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 43 V

Q104-1553-P
Vil = -0.5 V to 1.85 V
Vih = 2.23 V to 43 V.

15.6 Hardwired RT Address

Both boards provide Hardwired RT Addressing on the first channel. This operational mode is enabled by installing a shunt across JB2 and using the shared Avionics Discretes for setting the External RT Address.

15.7 Differential Triggers

Both boards have one differential trigger input (RS-485 0) and one differential trigger output (RS-485 1).

Output specs:

Vod (differential) = 2 V min into 50 Ω load, 5 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = $\pm$0.2 V max. with –20 V ≤ Vcm ≤ 25 V
Iin = 500 uA max @ Vin = 12 V, -400 uA max @ Vin = -7 V
Iin = 1000 uA max @ Vin = 25 V, -800 uA max @ Vin = -20 V
Rin = 24 KΩ min not taking into account Vneg_bias resistors.

15.8 Triggers

15.8.1 Pre-V6 Firmware, ISA & PCI Versions

Both boards have one differential trigger input (RS-485 0) and one differential trigger output (RS-485 1).

15.8.2 V6 Firmware, PCI Version Only

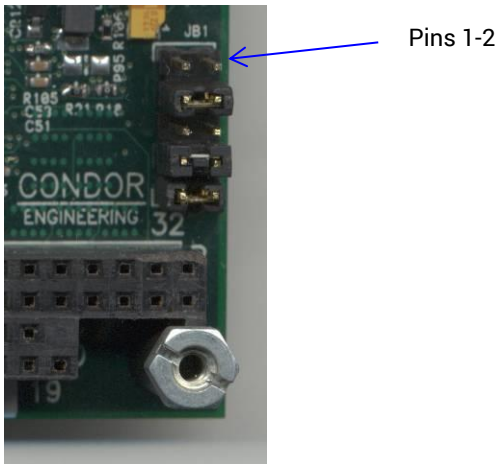
For the PCI board only, any Avionics discrete or differential can be programmed as a trigger input as well as a trigger output on a per-channel basis.

15.9 Q104-1553 (ISA) Memory Map

The Q104-1553 resides in ISA memory space in a host system. The board may be mapped into any available 16-KByte block in upper memory between segment addresses A000:0000 and E400:0000 (physical addresses A0000 to E4000 hexadecimal). The memory address is determined by the jumper settings on header JB1 (listed below). See the image of JB1 for pin 1 orientation.

The most significant address bit is located closest to the silkscreen 'JB1' on the circuit board. This corresponds to JB1 pins 1-2.

Figure 15-2 Q104 Jumper Block JB1



The Q104-1553 memory is paged by an internal page register, accessed at a word offset dedicated to each particular channel. (See the "MIL-STD-1553 Universal Core Architecture Reference Manual" for more information).

Table 15-2 Q104-1553 Memory Address Jumper Options

Selected Physical Address Range	JB1: 1-2	JB1: 3-4	JB1: 5-6	JB1: 7-8	JB1: 9-10
0A0000 - 0A3FFF	ON	OFF	ON	ON	ON
0A4000 - 0A7FFF	ON	OFF	ON	ON	OFF
0A8000 - 0ABFFF	ON	OFF	ON	OFF	ON
0AC000 - 0AFFFF	ON	OFF	ON	OFF	OFF
0B0000 - 0B3FFF	ON	OFF	OFF	ON	ON
0B4000 - 0B7FFF	ON	OFF	OFF	ON	OFF
0B8000 - 0BBFFF	ON	OFF	OFF	OFF	ON
0BC000 - 0BFFFF	ON	OFF	OFF	OFF	OFF
0C0000 - 0C3FFF	OFF	ON	ON	ON	ON
0C4000 - 0C7FFF	OFF	ON	ON	ON	OFF
0C8000 - 0CBFFF	OFF	ON	ON	OFF	ON
0CC000 - 0CFFFF	OFF	ON	ON	OFF	OFF
0D0000 - 0D3FFF	OFF	ON	OFF	ON	ON
0D4000 - 0D7FFF	OFF	ON	OFF	ON	OFF
0D8000 - 0DBFFF	OFF	ON	OFF	OFF	ON
0DC000 - 0DFFFF	OFF	ON	OFF	OFF	OFF
0E0000 - 0E3FFF	OFF	OFF	ON	ON	ON
0E4000 - 0E7FFF	OFF	OFF	ON	ON	OFF

15.9.1 Selecting Memory Addresses

Prior to selecting the memory block that the hardware is mapped into, the available system memory resources must be determined. For upper memory, the C800 and D000 segments (96 Kbytes) are allocated for adapter boards on the ISA platform. Before installing the board, an available 16-KByte block, starting at one of the base addresses listed in the table must be established.

When using any program to determine if a memory or I/O space is available for use, most only report what the operating system knows. If no operating system driver has been installed for a memory or I/O region, the program might report that it is available, even if some device is really using that region.

If multiple boards are being used in the same platform, then sufficient memory space must be available for each board. Two boards (up to eight 1553 channels) require 64K free bytes.

15.10 Q104-1553-P [PCI Interface] Memory Map – PCI Stack Locator

The Q104-1553-P resides in PCI memory space in a host system. While PCI devices are inherently Plug-and-Play, the mechanical implementation of the PC/104-*Plus* stack-through connector requires that the board be aware of its physical location in the PC/104-*Plus* stack for signal timing integrity. This is so that the card may observe the correct PCI clock, interrupt and IDSEL pins in the –*Plus* connector, those signals associated with a particular stack location. See the PC/104-*Plus* specification for complete details.

In general, the host card is located at the bottom of the PC/104-*Plus* stack. This is often referred to as Slot 0. The first –*Plus* add-in card is referred to Slot 1, while the next added card in the stack is designated Slot 2, and the stack grows upwards in this manner. The host adjusts clock trace lengths so that all cards see their PCI clock adjusted for no apparent skew.

NOTES

The PC/104-*Plus* specification makes no provisions for using more than four add-in *Plus* cards in a given system; although, several more ISA devices may be added on top.

Any non-*Plus* interface cards are typically installed on top of any –*Plus* cards.

Stack location is indicated to the Q104-P with the jumper block JB1. The most significant address bit is located closest to the silkscreen 'JB1' on the circuit board. This corresponds to JB1 pins 1-2.

Figure 15-3 Q104-P Jumper Block JB1

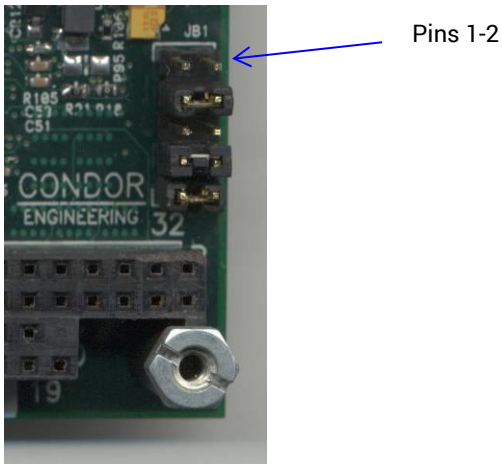


Table 15-3 PCI Stack Locator Jumpers

Slot Location	JB1: 7-8	JB1: 9-10
Slot 1	ON	ON
Slot 2	ON	OFF
Slot 3	OFF	ON
Slot 4	OFF	OFF

NOTE

An installed shunt indicates an active-low input signal to the clock selection circuitry.

The Q104-1553-P maps into an available 8-MByte memory window in PCI memory. See Figure 15-3 for pin 1 orientation.

15.11 PCI Interrupt Line Selection for the Q104-1553-P

Per the PC/104-*Plus* specification, the Q104-1553-P board includes jumper-selected interrupt line routing. In response to an enabled interrupt event, the board drives the interrupt corresponding to its slot location (i.e. INTA while installed in Slot 1, through INTD while installed in Slot 4). Consult the PC/104-*Plus* specification for details.

All channels on a Multi-channel Q104-1553-P board share the same hardware interrupt line, as selected above. The BusTools/1553-API handles sharing the interrupt between the channels

15.11.1 PCI Interrupt Override

To be compatible with certain legacy systems that do not correctly route interrupts, the Q104-1553-P may be operated in non-spec-compliant mode. To always route interrupts to PCI INTA, regardless of slot location, install a shunt at JB1:1-2 (jumper farthest from the J1 connector).

15.12 ISA Interrupt Line Selection for the Q104-1553 (IRQ3, 5, 7, 9-12, 14-15)

The Q104-1553 board features software-programmable interrupt line selection. There are no interrupt jumpers to set. An interrupt (not being used by another board) must be chosen.

The hardware interrupt number is selected when installing the software for 32-Bit Windows. Selecting “0” disables the hardware interrupts; the API defaults to polling the board. The Linux installation uses 7 as the default IRQ.

16 • R15-USB Installation

16.1 R15-USB Installation Procedure

This section describes installation of the R15-USB. The R15-USB is a USB-to-MIL-STD-1553 adapter and is available in dual- and multi-function configurations.

16.1.1 Hardware Installation

Follow these steps to install the hardware:

1. Remove the unit from its packaging.
2. After the software installation, attach the R15-USB to a USB port on the host computer using a standard USB cable.
3. Connect the MIL-STD-1553 bus to the appropriate connectors on the R15-USB.

16.2 R15-USB

Figure 16-1 R15-USB Front View

Figure 16-2 R15-USB Rear View

16.3 Status LEDs

There are four status LEDs on the R15-USB:

- **CONFIG** – Indicates that the R15-USB has been successfully configured.
- **EXT PWR** – Indicates that the R15-USB is being powered by external power from the +5VDC input on the 15-pin d-subminiature connector.
- **CH1 / CH2 ACTIVE** – Illuminates on detection of traffic on the applicable 1553 channel.

16.4 R15-USB Connector Description

The USB interface is a standard series “B” receptacle connector with screw-lock capability. MIL-STD-1553 I/O is provided by standard tri-axial 1553 MIL-STD-1553 connectors. All other I/O is routed to a 15 pin D-subminiature plug connector.

16.4.1 R15-USB Pin Assignments (15 pin plug D-Subminiature)

Table 16-1 specifies the I/O connector pin assignments for the 15-pin D-subminiature connector (plug).

Table 16-1 R15-USB I/O Pin Assignments

Pin	Signal
1	IRIG RX+
2	IRIG TX
3	RETURN (GND)
4	Discrete 7
5	Discrete 5
6	Discrete 3
7	Discrete 1
8	+5VDC IN 5.0 +/- 5%, up to 1A (See Note)
9	IRIG RX-
10	RETURN (GND)
11	Discrete 8
12	Discrete 6
13	Discrete 4
14	Discrete 2
15	RETURN (GND)

NOTE

The input on pin #8 is only needed if the USB port is not able to supply sufficient current.

16.5 Triggers

Any of the eight discrete inputs may be programmed as a trigger input or output for each channel.

16.6 Hardwired RT Address

The R15-USB does not provide Hardwired RT address inputs. If the RT address needs to be defined by the connector, any six of the eight discretes may be used to define an RT address. The user can read the discretes register to determine the RT address and then program the RT to respond to that address.

16.7 IRIG Signaling

IRIG time may be received on the signals “IRIG RX+” and “IRIG RX-“.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 KΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.5 V - Zout drop
Voh_min = 2.7 V min - Zout drop
Vol = 0.4 V max + Zout drop @ 4 ma
Iol / Ioh = 4 mA max
Zout = 392 Ω output series resistance.

16.8 Avionics Discrete I/O

Eight discrete I/O signals (Discrete X) are available.

Output specs:

Open drain output with Vds = 60 V max.
Vol = 0.35 V max @ Iol = 500 mA.

Input specs:

Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 60 V max
Vil = -0.5 V to 1.8 V
Vih = 2.2 V to 60 V.

17 • RAR15-XMC Installation

17.1 Installation Procedure

This section tells how to install the RAR15-XMC board. The RAR15-XMC is a low-power, single-lane PCIe XMC based multi-protocol product offering a maximum channel count of four 1553 channels, 18 ARINC 429 receive channels, eight ARINC 429 transmit channels in addition to various discrete, IRIG, external clocking, triggering options and I/O options.

17.1.1 Hardware Installation

After installing the software, follow the steps below to install the hardware. The RAR15-XMC installs in XMC.3 [PCI Express only] sites.

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Insert the RAR15-XMC into the XMC site.

NOTE

I/O for the RAR15-XMC is available from either the P14 (PMC) or P16 (XMC) rear I/O connectors, Figure 17-1 shows both configurations for illustration purposes only.

17.2 RAR15-XMC

Figure 17-1 RAR15-XMC

17.3 RAR15-XMC Part Number Description

The RAR15-XMC has several configurations available. The 1553 channels are available as multi-function (concurrent BC, RT, BM operation allowed) or as dual-function (concurrent BC, BM or RT, BM operation allowed). The italicized “n” in the part number denotes either multi-function (M) or dual-function (D). The leading ”R” denotes a RoHS product. The board is also available in a non-RoHS build, in these

cases the leading “R” is omitted (e.g. AR15-XMC). Part numbers with an “-IT” suffix denote boards rated for an industrial temperature range (-40° C to +85° C) while an “-XT” suffix denotes boards with an extended temperature range (-40° C to +95° C). In both cases the range is applicable to the temperature at the primary thermal interface of the XMC board as defined in ANSI/VITA 20-2001 (R2005).

NOTE

The “-XT” suffix is no longer an available option.

Table 17-1 RAR15-XMC Part Number Description

RAR15XMC	I/O	1553 Channels	429 RX Channels	429 TX Channels	Discrete I/O
-1084*n*C1	P16	1-4	1-10	1-8	7-12
-1084*n*C3	P14	1-4	1-10	1-8	0
-1042*n*C1	P16	1-2	1-10	1-4	1-12
-1042*n*C3	P14	1-2	1-10	1-4	1-6

17.4 Status LEDs

There are up to five LEDs on the board, one bi-colored LED for status of each 1553 channel and a single green LED for configuration and link status:

- **CH 1, CH 2, CH3, CH4 – 1553 Bus Activity –** These status indicators consist of co-packaged green and red LEDs for each 1553 channel, the green LED will flash briefly with each 1553 message received or transmitted by the channel, the red LED will turn on whenever the channel is configured to run traffic internally.
- **CONF/LINK** – This green LED turns on upon successful FPGA configuration from an onboard configuration device and flashes under normal conditions when the PCIe link is active.

17.5 RAR15-XMC Connector Description

17.5.1 RAR15-XMC Signal Description

Access and function of several RAR15-XMC connector pins are shared. The function of the pin is dependent on the configuration ordered. Table 17-2 lists the primary and alternate functions of the pins.

Table 17-2 RAR15-XMC Primary/Alternate Pin Functions

Signal Name	Primary Function	Alternate Function
1553_CH*n*A+	MIL-STD-1553 bus A "+", *n*=1-4	none
1553_CH*n*A-	MIL-STD-1553 bus A "-", *n*=1-4	none
1553_CH*n*B+	MIL-STD-1553 bus B "+", *n*=1-4	none
1553_CH*n*B-	MIL-STD-1553 bus B "-", *n*=1-4	none
429_RX*n*_A	ARINC 429 receive "A" input, *n*=1-8	none
429_RX*n*_B	ARINC 429 receive "B" input, *n*=1-8	none
429_RX*n+10*_TX*n*_A	ARINC 429 transmit "A" output, *n*=1-6	ARINC 429 receive "A" input, *n*=1-6
429_RX*n+10*_TX*n*_B	ARINC 429 transmit "B" output, *n*=1-6	ARINC 429 receive "B" input, *n*=1-6
429_RX*n+10*_TX*n*_A/DIS*x*	ARINC 429 transmit "A" output, *n*=5-7, *x*= 1-6	ARINC 429 receive "A" input, *n*=1-6 or Avionic Discrete
429_RX*n+10*_TX*n*_B/DIS*x*	ARINC 429 transmit "B" ouput, *n*=5-7, *x*= 1-6	ARINC 429 receive "B" input, *n*=1-6 or Avionic Discrete
429_RX18_TX8_A/IRIGTX	ARINC 429 Ch. 8 transmit "A" output	ARINC 429 Ch. 18 receive "A" input or IRIG Transmit
429_RX18_TX8_B/IRIG_IN-	ARINC 429 Ch. 8 transmit "B" output	ARINC 429 Ch. 18 receive "B" input or "-" input for differential IRIG
429_RX9_A/TRIG_IN_CH1	ARINC 429 Ch. 9 receive "A" input	Trigger input for 1553 channel 1
429_RX9_B/TRIG_IN_CH2	ARINC 429 Ch. 9 receive "B" input	Trigger input for 1553 channel 2
429_RX10_A/TRIG_IN_CH3	ARINC 429 Ch. 10 receive "A" input	Trigger input for 1553 channel 3
429_RX10_B/TRIG_IN_CH4	ARINC 429 Ch. 10 receive "B" input	Trigger input for 1553 channel 4
IRIG_IN+	IRIG receive "+" input or IRIG input for single ended configurations	none
RTAD*n*	Base RT Address, *n*= 1-5	none
RTADPTY	Base RT Address Parity Bit	none
DISCRETE*n*	Avionic Discrete, *n*= 7-12	None (P16 only)
EXT_CLK+/DIS7	Timer external clock "+" differential input	Avionic Discrete 7 (P14 only)
EXT_CLK-/DIS8	Timer external clock "-" differential input	Avionic Discrete 8 (P14 only)
EXT_RST+/DIS9	Timer external reset "+" differential input	Avionic Discrete 9 (P14 only)
EXT_RST-/DIS10	Timer external reset "-" differential input	Avionic Discrete 10 (P14 only)

17.5.2 RAR15-XMC I/O Connector Generic Assignments

The RAR15-XMC uses either P14 (PMC) or P16 (XMC) for all I/O signals. The following tables show the generic pin assignments for P14 & P16 I/O board.

Table 17-3 RAR15-XMC P14 PMC I/O Connector Generic Pin Assignments

Function	Pin	Pin	Function
429_RX7_A	1	2	429_RX7_B
429_RX8_A	3	4	429_RX8_B
429_RX13_TX3_A	5	6	429_RX13_TX3_B
429_RX14_TX4_A	7	8	429_RX14_TX4_B
1553_CH1A+	9	10	1553_CH1A-
1553_CH2A+	11	12	1553_CH2A-
1553_CH1B+	13	14	1553_CH1B-
IRIG_IN+	15	16	GND
1553_CH2B+	17	18	1553_CH2B-
429_RX1_A	19	20	429_RX1_B
429_RX18_TX8_A/IRIG	21	22	429_RX18_TX8_B/IRIG_IN-
429_RX2_A	23	24	429_RX2_B
429_RX9_A/TRIG_IN_C	25	26	429_RX9_B/TRIG_IN_CH2
1553_CH3A+	27	28	1553_CH3A-
RTAD0	29	30	RTAD1
1553_CH4A+	31	32	1553_CH4A-
429_RX10_A/TRIG_IN_	33	34	429_RX10_B/TRIG_IN_CH4
1553_CH3B+	35	36	1553_CH3B-
RTAD2	37	38	RTAD3
1553_CH4B+	39	40	1553_CH4B-
429_RX17_TX7_A/DIS	41	42	429_RX17_TX7_B/DIS6
429_RX3_A	43	44	429_RX3_B
RTAD4	45	46	RTADPTY
429_RX4_A	47	48	429_RX4_B
EXT_CLK+/DIS7	49	50	EXT_CLK-/DIS8
429_RX5_A	51	52	429_RX5_B
429_RX15_TX5_A/DIS	53	54	429_RX15_TX5_B/DIS2
429_RX6_A	55	56	429_RX6_B
EXT_RST+/DIS9	57	58	EXT_RST-/DIS10
429_RX11_TX1_A	59	60	429_RX11_TX1_B
429_RX16_TX6_A/DIS	61	62	429_RX16_TX6_B/DIS4
429_RX12_TX2_A	63	64	429_RX12_TX2_B

Table 17-4 RAR15-XMC P16 XMC I/O Connector Generic Pin Assignments

	a	b	c	d	e	f
1	429_RX7_A	429_RX7_B	N/A	429_RX8_A	429_RX8_B	N/A
2	GND	GND	N/A	GND	GND	N/A
3	429_RX13_TX3_A	429_RX13_TX3_B	N/A	429_RX14_ TX4_A	429_RX14_ TX4_B	N/A
4	GND	GND	N/A	GND	GND	N/A
5	1553_CH1A+	1553_CH1A-	EXT_CLK+	1553_CH2A+	1553_CH2A-	EXT_RST+
6	GND	GND	EXT_CLK-	GND	GND	EXT_RST-
7	1553_CH1B+	1553_CH1B-	429_RX18_ TX8_A/IRIGTX	1553_CH2B+	1553_CH2B-	GND
8	GND	GND	IRIG_IN+	GND	GND	429_RX9_A /TRIG_IN_CH1
9	429_RX1_A	429_RX1_B	429_RX18_ TX8_B/IRIG_IN-	429_RX2_A	429_RX2_B	429_RX9_B /TRIG_IN_CH2
10	GND	GND	RTAD0	GND	GND	429_RX10_A /TRIG_IN_CH3
11	1553_CH3A+	1553_CH3A-	RTAD1	1553_CH4A+	1553_CH4A-	429_RX10_B /TRIG_IN_CH4
12	GND	GND	RTAD2	GND	GND	429_RX17_ TX7_A/DIS5
13	1553_CH3B+	1553_CH3B-	RTAD3	1553_C-H4B+	1553_CH4B-	429_RX17_ TX7_B/DIS6
14	GND	GND	RTAD4	GND	GND	DISCRETE7
15	429_RX3_A	429_RX3_B	RTADPTY	429_RX4_A	429_RX4_B	DISCRETE8
16	GND	GND	429_RX15_ TX5_A/DIS1	GND	GND	DISCRETE9
17	429_RX5_A	429_RX5_B	429_RX15_ TX5_B/DIS2	429_RX6_A	429_RX6_B	DISCRETE10
18	GND	GND	429_RX16_ TX6_A/DIS3	GND	GND	DISCRETE11
19	429_RX11_TX1_A	429_RX11_TX1_B	429_RX16_ TX6_B/DIS4	429_RX12_ TX2_A	429_RX12_ TX2_B	DISCRETE12

17.5.3 RAR15-XMC Model Specific I/O Connector Assignments

The following tables show the pin assignments for RAR15-XMC boards with specific part numbers.

Table 17-5 RAR15-XMC-1084nC1 P16 XMC I/O Pin Assignments

	a	b	c	d	e	f
1	429_RX7_A	429_RX7_B	N/A	429_RX8_A	429_RX8_B	N/A
2	GND	GND	N/A	GND	GND	N/A
3	429_TX3_A	429_TX3_B	N/A	429_TX4_A	429_TX4_B	N/A
4	GND	GND	N/A	GND	GND	N/A
5	1553_CH1A+	1553_CH1A-	EXT_CLK+	1553_CH2A+	1553_CH2A-	EXT_RST+
6	GND	GND	EXT_CLK-	GND	GND	EXT_RST-
7	1553_CH1B+	1553_CH1B-	429_TX8_A	1553_CH2B+	1553_CH2B-	GND
8	GND	GND	IRIG_IN+	GND	GND	429_RX9_A
9	429_RX1_A	429_RX1_B	429_TX8_B	429_RX2_A	429_RX2_B	429_RX9_B
10	GND	GND	RTAD0	GND	GND	429_RX10_A
11	1553_CH3A+	1553_CH3A-	RTAD1	1553_CH4A+	1553_CH4A-	429_RX10_B
12	GND	GND	RTAD2	GND	GND	429_TX7_A
13	1553_CH3B+	1553_CH3B-	RTAD3	1553_C-H4B+	1553_CH4B-	429_TX7_B
14	GND	GND	RTAD4	GND	GND	DISCRETE7
15	429_RX3_A	429_RX3_B	RTADPTY	429_RX4_A	429_RX4_B	DISCRETE8
16	GND	GND	429_TX5_A	GND	GND	DISCRETE9
17	429_RX5_A	429_RX5_B	429_TX5_B	429_RX6_A	429_RX6_B	DISCRETE10
18	GND	GND	429_TX6_A	GND	GND	DISCRETE11
19	429_TX1_A	429_TX1_B	429_TX6_B	429_TX2_A	429_TX2_B	DISCRETE12

Table 17-6 RAR15-XMC-1042nC1 P16 XMC I/O Pin Assignments

	a	b	c	d	e	f
1	429_RX7_A	429_RX7_B	N/A	429_RX8_A	429_RX8_B	N/A
2	GND	GND	N/A	GND	GND	N/A
3	429_TX3_A	429_TX3_B	N/A	429_TX4_A	429_TX4_B	N/A
4	GND	GND	N/A	GND	GND	N/A
5	1553_CH1A+	1553_CH1A-	EXT_CLK+	1553_CH2A+	1553_CH2A-	EXT_RST+
6	GND	GND	EXT_CLK-	GND	GND	EXT_RST-
7	1553_CH1B+	1553_CH1B-	N/A	1553_CH2B+	1553_CH2B-	GND
8	GND	GND	IRIG_IN+	GND	GND	429_RX9_A
9	429_RX1_A	429_RX1_B	N/A	429_RX2_A	429_RX2_B	429_RX9_B
10	GND	GND	RTAD0	GND	GND	429_RX10_A
11	N/A	N/A	RTAD1	N/A	N/A	429_RX10_B
12	GND	GND	RTAD2	GND	GND	DISCRETE5
13	N/A	N/A	RTAD3	N/A	N/A	DISCRETE6
14	GND	GND	RTAD4	GND	GND	DISCRETE7
15	429_RX3_A	429_RX3_B	RTADPTY	429_RX4_A	429_RX4_B	DISCRETE8
16	GND	GND	DISCRETE1	GND	GND	DISCRETE9
17	429_RX5_A	429_RX5_B	DISCRETE2	429_RX6_A	429_RX6_B	DISCRETE10
18	GND	GND	DISCRETE3	GND	GND	DISCRETE11
19	429_TX1_A	429_TX1_B	DISCRETE4	429_TX2_A	429_TX2_B	DISCRETE12

Table 17-7 RAR15-XMC-1084nC3 P14 XMC I/O Pin Assignments

Function	Pin	Pin	Function
429_RX7_A	1	2	429_RX7_B
429_RX8_A	3	4	429_RX8_B
429_ TX3_A	5	6	429_TX3_B
429_ TX4_A	7	8	429_ TX4_B
1553_CH1A+	9	10	1553_CH1A-
1553_CH2A+	11	12	1553_CH2A-
1553_CH1B+	13	14	1553_CH1B-
IRIG_IN+	15	16	GND
1553_CH2B+	17	18	1553_CH2B-
429_RX1_A	19	20	429_RX1_B
429_ TX8_A	21	22	429 _TX8_B
429_RX2_A	23	24	429_RX2_B
429_RX9_A	25	26	429_RX9_B
1553_CH3A+	27	28	1553_CH3A-
RTAD0	29	30	RTAD1
1553_CH4A+	31	32	1553_CH4A-
429_RX10_A	33	34	429_RX10_B
1553_CH3B+	35	36	1553_CH3B-
RTAD2	37	38	RTAD3
1553_CH4B+	39	40	1553_CH4B-
429_TX7_A	41	42	429_ TX7_B
429_RX3_A	43	44	429_RX3_B
RTAD4	45	46	RTADPTY
429_RX4_A	47	48	429_RX4_B
EXT_CLK+	49	50	EXT_CLK-
429_RX5_A	51	52	429_RX5_B
429_ TX5_A	53	54	429_TX5_B
429_RX6_A	55	56	429_RX6_B
EXT_RST+	57	58	EXT_RST+
429_TX1_A	59	60	429_TX1_B
429_TX6_A	61	62	429_TX6_B
429_TX2_A	63	64	429_TX2_B

Table 17-8 RAR15-XMC-1042nC3 P14 XMC I/O Pin Assignments

Function	Pin	Pin	Function
429_RX7_A	1	2	429_RX7_B
429_RX8_A	3	4	429_RX8_B
429_TX3_A	5	6	429_TX3_B
429_TX4_A	7	8	429_TX4_B
1553_CH1A+	9	10	1553_CH1A-
1553_CH2A+	11	12	1553_CH2A-
1553_CH1B+	13	14	1553_CH1B-
IRIG_IN+	15	16	GND
1553_CH2B+	17	18	1553_CH2B-
429_RX1_A	19	20	429_RX1_B
N/A	21	22	N/A
429_RX2_A	23	24	429_RX2_B
429_RX9_A	25	26	429_RX9_B
N/A	27	28	N/A
RTAD0	29	30	RTAD1
N/A+	31	32	N/A
429_RX10_A	33	34	429_RX10_B
N/A	35	36	N/A
RTAD2	37	38	RTAD3
N/A	39	40	N/A
DISCRETE5	41	42	DISCRETE6
429_RX3_A	43	44	429_RX3_B
RTAD4	45	46	RTADPTY
429_RX4_A	47	48	429_RX4_B
EXT_CLK+	49	50	EXT_CLK-
429_RX5_A	51	52	429_RX5_B
DISCRETE1	53	54	DISCRETE2
429_RX6_A	55	56	429_RX6_B
EXT_RST+	57	58	EXT_RST+
429_TX1_A	59	60	429_TX1_B
DISCRETE3	61	62	DISCRETE4
429_TX2_A	63	64	429_TX2_B

17.5.4 RAR15-XMC Host Interface Connector Description

The P15 connector implements a one-lane PCIe XMC.3 bus interface to the host as described in ANSI/VITA42.3.

Table 17-9 RAR15-XMC P15 XMC Connector Pin Assignments

	a	b	c	d	e	f
1	PET0p0	PET0n0	N/A	N/A	N/A	VPWR
2	GND	GND	N/A	GND	GND	MRSTI#
3	N/A	N/A	N/A	N/A	N/A	VPWR
4	GND	GND	N/A	GND	GND	N/A
5	N/A	N/A	N/A	N/A	N/A	VPWR
6	GND	GND	N/A	GND	GND	N/A
7	N/A	N/A	N/A	N/A	N/A	VPWR
8	GND	GND	TDI	GND	GND	N/A
9	N/A	N/A	N/A	N/A	N/A	VPWR
10	GND	GND	TD0	GND	GND	N/A
11	PER0p0	PER0n0	N/A	N/A	N/A	VPWR
12	GND	GND	N/A	GND	GND	N/A
13	N/A	N/A	N/A	N/A	N/A	VPWR
14	GND	GND	N/A	GND	GND	N/A
15	N/A	N/A	N/A	N/A	N/A	VPWR
16	GND	GND	MVMRO	GND	GND	N/A
17	N/A	N/A	N/A	N/A	N/A	N/A
18	GND	GND	N/A	GND	GND	N/A
19	REFCLK+0	REFCLK-0	N/A	N/A	N/A	N/A

17.6 Triggers

Depending on the configuration ordered, each 1553 channel may have a dedicated Trigger Input signal. The differential clock input and time-tag reset signals can be used as trigger outputs if not used as inputs.

Input specs for the dedicated single-ended trigger input if available is:

Input specs:

Input interally pulled to 3.3V via 10 KΩ series resistor and protection diode.
Input range -0.5 to 27 V max.
Vil = -0.5 V to 0.8 V
Vih = 1.7 V to 27 V

17.7 IRIG Signaling

IRIG time may be received on the signal IRIG IN + on boards configured with a single-ended IRIG input (standard for the RAR15-XMC-IT) and on both the IRIG IN+ and IRIG IN – signals on boards configured with differential IRIG inputs. When enabled by the software (and available on the board), IRIG TX transmits IRIG B002 data from the onboard IRIG encoder. When available, the IRIG OUT signal can source/sink 16 mA at valid TTL levels.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.6 V min - Zout drop
Vol = 0.4 V max + Zout drop
Iol / Ioh = 12 mA max
Zout = 49.9 Ω output series resistance.

17.8 Avionics Discrete I/O

Twelve Avionics Discrete signals are provided. These discrete signals may also be assigned as input and output triggers.

Output specs:

Open drain output with Vds = 60 V max.
Vol = 0.35 V max @ Iol = 500 mA.

Input specs:

Input interally pulled to 3.3V via 10 KΩ after input protection diode.
Input range -0.5 to 60 V max
Vil = -0.5 V to 2.4 V
Vih = 3.0 V to 60 V.

17.9 Differential I/O

A differential clock input and a differential time-tag reset input is provided. The differential clock input accepts a 1 MHz - 10 MHz external clock input (under software control). The reset input resets the card's time tag to zero upon receipt of a valid (greater than 50 ns positive pulse) input signal. The inputs are compatible with TIA/EIA-485-A specifications. They can be used single-ended as well since the negative terminal is biased at ~ 1.9V.

Output specs:

Vod (differential) = 2 V min into 50 Ω load, 3.3 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 125 uA max @ Vin = 12 V, -100 uA max @ Vin = -7 V
Rin = 96 KΩ min not taking into account Vneg_bias resistors.

Negative pin bias:

Vneg_bias = ~1.9 V via 10 KΩ pull-up to 3.3V and 13.7 KΩ pull-down to ground.

17.10 Hardwired RT Address

Each 1553 channel present on the RAR15XMC-XT can be individually configured to provide hardwired RT addressing.

Input specs:

Input range -0.3 to 5.5 V max.
Input pulled to 5V via 866Ω

17.11 Flash Configurable 1553 Options

The RAR15XMC-XT has 1553 channel options that may be individually configured by the user on a per-channel basis using the Abaco Flash Configurable Programmer Windows utility.

Table 17-10 Flash Configurable 1553 Options

Channel Option	Description	Default
RT Offset Value	Valid entries are 0-31	0
1760 Startup	Enables or disables 1760 response	Disabled
HWRT Mode	RT Address = Offset or Offset + Hardwire RT address	Offset + Hardwire RT Address
Enforce BM Only	When enabled will not permit BC or RT operation.	Disabled
Startup Coupling	Indicates 1553 bus coupling which on the RAR15-XMC board is fixed.	Transformer
A/B Startup	Selects Mil-STD-1553A or B protocol	1553B
Single Validated RT	When SRT is selected the channel functions as a single validated RT and as a BM. In Standard Mode the board has Dual or Multi-function, depending on what was purchased.	Standard

17.12 Memory

The RAR15XMC-XT requires a 16-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

The board has 8 MBytes of volatile RAM (GSI P/N GSI8642Z36GB-250M) and 32 or 64 Mbits of non-volatile flash memory (Winbond P/N W25Q32BVSSAG or W25Q32BVSSAG – supply-dependent) used for board and FPGA configuration. This non-volatile flash memory is not accessible for general purpose use and is only accessible through the Abaco Flash Configurable Programmer software utility.

Flash memory can be write protected in either of two ways, in-system or flash based:

- **In System**: The active high assertion of the XMC MVMRO write prohibit signal on the P15 connector prevents flash from being written to in-system however, if the MVMRO is un-asserted or the board placed in another system where the MVMRO signal is not asserted flash may once again be written to.
- **Flash Based:** The flash based method requires enabling the Write Protect Board Option through the Abaco Flash Config Programmer Windows utility. Once this bit in enabled and board power is cycled the flash cannot be written to again without being returned to the factory for reprogramming.

17.13 Mechanical and Power

- Weight: 84 grams or 2.96 oz. (RAR15XMC-1084MC1, non-coated)
- Size: Single-width XMC mezzanine card conforming to the standard IEEE 1386-2001 form factor (143.75 mm x 74 mm)
- Power (Supplied through the XMC P15 VPWR pins): +5 V or +12 V

- Power (All channels terminated and transmitting at 25% duty cycle): 4.5 W (VPWR= +5 V)

18 • RAR15XF Installation

NOTE

If you purchased the RAR15XF-TB variant of this product, please also refer to the “TB3-TO-CMC-LP Thunderbolt™ 3 Expansion Adapter User's Guide” provided with the product or also available on the Abaco website (https://www.abaco.com/TB3LP_Guide). This document contains important additional information for operating in a Thunderbolt environment.

18.1 Installation Procedure

This section tells how to install the RAR15XF board. The RAR15XF is a low-power, single-lane PCIe XMC based multi-protocol product offering a maximum channel count of four 1553 channels, 10 ARINC 429 receive channels, eight fully bi-directional ARINC 429 transmit/receive channels in addition to various discrete, IRIG, external clocking, triggering options and I/O options.

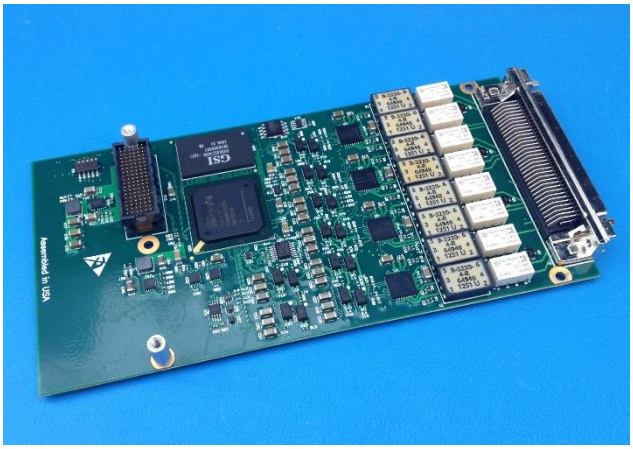
18.1.1 Hardware Installation

After installing the software, follow the steps below to install the hardware. The RAR15XF installs in XMC.3 [PCI Express only] sites.

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Insert the RAR15XF into the XMC site.

18.2 RAR15XF

Figure 18-1 RAR15XF



18.3 RAR15XF Part Number Description

The RAR15XF has several configurations available; the 1553 channels are available as multi-function (concurrent BC, RT, BM operation allowed) or as dual-function

(concurrent BC, BM or RT, BM operation allowed). The italicized "*n*" in the part number denotes either multi-function (M) or dual-function (D). The leading "R" denotes a RoHS product, the board is also available in a non-RoHS build, in these cases the leading "R" is omitted (e.g. AR15XF).

Table 18-1 RAR15-XMC Part Number Description

RAR15XF	I/O	1553 Channels	429 RX Channels	429 TX Channels	Discrete I/O
-1084*n*	P1 (front)	1-4	1-10	1-8	7-12
-1042*n*		1-2	1-10	1-4	1-12

18.4 Status LEDs

There are up to five LEDs on the board, one bi-colored LED for status of each 1553 channel and a single green LED for configuration and link status:

- **CH 1, CH 2, CH3, CH4 – 1553 Bus Activity –** These status indicators consist of co-packaged green and red LEDs for each 1553 channel, the green LED will flash briefly with each 1553 message received or transmitted by the channel, the red LED will turn on whenever the channel is configured to run traffic internally.
- **CONF/LINK** – This green LED turns on upon successful FPGA configuration from an onboard configuration device and flashes under normal conditions when the PCIe link is active.

18.5 RAR15XF Connector Description

18.5.1 RAR15XF Signal Description

Access and function of several RAR15XF connector pins are shared. The function of the pin is dependent on the configuration ordered (indicated as "standard" or "option"). The following table lists the primary and alternate functions of the pins.

Table 18-2 RAR15XF Primary/Alternate Pin Functions

Signal Name	Primary Function	Alternate Function
1553_CH*n*A+	MIL-STD-1553 bus A "+", *n*=1-4	none
1553_CH*n*A-	MIL-STD-1553 bus A "-", *n*=1-4	none
1553_CH*n*B+	MIL-STD-1553 bus B "+", *n*=1-4	none
1553_CH*n*B-	MIL-STD-1553 bus B "-", *n*=1-4	none
429_RX*n*_A	ARINC 429 receive "A" input, *n*=1-8	none
429_RX*n*_B	ARINC 429 receive "B" input, *n*=1-8	none
429_RX*n+10*_TX*n*_A	ARINC 429 receive "A" input ARINC 429 transmit "A" output, *n*=1-6	none

Signal Name	Primary Function	Alternate Function
429_RX*n+10*_TX*n*_B	ARINC 429 receive “B” input ARINC 429 transmit “B” output, *n*=1-6	none
429_RX*n+10*_TX*n*_A/DIS*x*	ARINC 429 receive “A” input ARINC 429 transmit “A” output, *n*=5-7	Avionic Discrete, *x*= 1-5 odd
429_RX*n+10*_TX*n*_B/DIS*x*	ARINC 429 receive “B” input ARINC 429 transmit “B” ouput, *n*=5-7	Avionic Discrete, *x*= 2-6 even
429_RX9_A/TRIG_IN_CH1	ARINC 429 Ch. 9 receive “A” input (standard)	TTL Trigger input for 1553 channel 1 (option)
429_RX9_B/TRIG_IN_CH2	ARINC 429 Ch. 9 receive “B” input (standard)	TTL Trigger input for 1553 channel 2 (option)
429_RX10_A/TRIG_IN_CH3	ARINC 429 Ch. 10 receive “A” input (standard)	TTL Trigger input for 1553 channel 3 (option)
429_RX10_B/TRIG_IN_CH4	ARINC 429 Ch. 10 receive “B” input (standard)	TTL Trigger input for 1553 channel 4 (option)
IRIG_IN+	IRIG receive “+” input	none
IRIG_IN-	IRIG receive “-” input (connected this pin to ground if single ended IRIG input used)	none
IRIG_TX	IRIG generator output	none
DISCRETE 7/RTAD0	Discrete bit 7	Hardwire RT address bit 0
DISCRETE 8/RTAD1	Discrete bit 8	Hardwire RT address bit 1
DISCRETE 9/RTAD2	Discrete bit 9	Hardwire RT address bit 2
DISCRETE 10/RTAD3	Discrete bit 10	Hardwire RT address bit 3
DISCRETE 11/RTAD4	Discrete bit 11	Hardwire RT address bit 4
DISCRETE 12/RTADPTY	Discrete bit 12	Hardwire RT address parity
EXT_CLK+	Timer external clock “+” differential input	none
EXT_CLK-	Timer external clock “-” differential input	none
EXT_RST+	Timer external reset “+” differential input	none
EXT_RST-	Timer external reset “-” differential input	none

18.5.2 RAR15XF I/O Connector Generic Assignments

The RAR15XF uses P1 for all I/O signals, a 68-pin SCSI III receptacle type connector. It’s mate would be a TE Connectivity 1-5750913-7 or equivalent.

Table 18-3 RAR15XF P1 Front I/O Connector Pin Assignments

Pin	Function	Pin	Function
1	1553_CH4B+	35	1553_CH4B-
2	1553_CH4A+	36	1553_CH4A-
3	429_RX1_A	37	429_RX1_B
4	429_RX2_A	38	429_RX2_B

Pin	Function
5	429_RX3_A
6	429_RX4_A
7	429_RX5_A
8	429_RX6_A
9	429_RX7_A
10	429_RX8_A
11	1553_CH3B+
12	1553_CH3A+
13	429_RX9_A/TRIG_IN_CH1
14	429_RX10_A/TRIG_IN_CH3
15	GND
16	429_RX11_TX1_A
17	429_RX12_TX2_A
18	429_RX13_TX3_A
19	429_RX14_TX4_A
20	429_RX15_TX5_A/DIS_1
21	429_RX16_TX6_A/DIS_3
22	429_RX17_TX7_A/DIS_5
23	429_RX18_TX8_A
24	IRIG_IN+
25	1553_CH2B+
26	1553_CH2A+
27	IRIG_TX
28	EXTCLK+
29	EXTRST+
30	DISCRETE 7/RTAD0
31	DISCRETE 9/RTAD2
32	DISCRETE 11/RTAD4
33	1553_CH1B+
34	1553_CH1A+

Pin	Function
39	429_RX3_B
40	429_RX4_B
41	429_RX5_B
42	429_RX6_B
43	429_RX7_B
44	429_RX8_B
45	1553_CH3B-
46	1553_CH3A-
47	429_RX9_B/TRIG_IN_CH2
48	429_RX10_B/TRIG_IN_CH3
49	GND
50	429_RX11_TX1_B
51	429_RX12_TX2_B
52	429_RX13_TX3_B
53	429_RX14_TX4_B
54	429_RX15_TX5_B/DIS_2
55	429_RX16_TX6_B/DIS_4
56	429_RX17_TX7_B/DIS_6
57	429_RX18_TX8_B
58	IRIG_IN-
59	1553_CH2B-
60	1553_CH2A-
61	GND
62	EXTCLK-
63	EXTRST-
64	DISCRETE 8/RTAD1
65	DISCRETE 10/RTAD3
66	DISCRETE 12/RTADPTY
67	1553_CH1B-
68	1553_CH1A-

18.5.3 RAR15XF Transition Cable

Separate Transition Cable assemblies are provided with two and four-channel boards. Cable information and pinouts for the transition cables are provided in the Appendix A RCONRAR15-X section.

18.5.4 RAR15XF Host Interface Connector Description

The P15 connector implements a one-lane PCIe XMC.3 bus interface to the host as described in ANSI/VITA42.3.

Table 18-4 RAR15XF P15 XMC Connector Pin Assignments

	a	b	c	d	e	f
1	PET0p0	PET0n0	N/A	N/A	N/A	VPWR
2	GND	GND	N/A	GND	GND	MRSTI#
3	N/A	N/A	N/A	N/A	N/A	VPWR
4	GND	GND	N/A	GND	GND	N/A
5	N/A	N/A	N/A	N/A	N/A	VPWR
6	GND	GND	N/A	GND	GND	N/A
7	N/A	N/A	N/A	N/A	N/A	VPWR
8	GND	GND	TDI	GND	GND	N/A
9	N/A	N/A	N/A	N/A	N/A	VPWR
10	GND	GND	TD0	GND	GND	N/A
11	PER0p0	PER0n0	N/A	N/A	N/A	VPWR
12	GND	GND	N/A	GND	GND	N/A
13	N/A	N/A	N/A	N/A	N/A	VPWR
14	GND	GND	N/A	GND	GND	N/A
15	N/A	N/A	N/A	N/A	N/A	VPWR
16	GND	GND	MVMRO	GND	GND	N/A
17	N/A	N/A	N/A	N/A	N/A	N/A
18	GND	GND	N/A	GND	GND	N/A
19	REFCLK+0	REFCLK-0	N/A	N/A	N/A	N/A

18.6 Triggers

Depending on the configuration ordered, each 1553 channel may have a dedicated Trigger Input signal. The differential clock input and time-tag reset signals can be used as trigger outputs if not used as inputs.

18.7 IRIG Signaling

IRIG time may be received on the IRIG IN+ and IRIG IN – signals on boards configured with differential IRIG inputs. When enabled by the software, IRIG TX transmits IRIG B002 data from the onboard IRIG encoder.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.6 V - Zout drop
Voh_min = 2.6 V min - Zout drop
Vol = 0.4 V max + Zout drop
Iol / Ioh = 12 mA max
Zout = 99.8 Ω output series resistance.

18.8 Avionics Discrete I/O

Up to twelve Avionics Discrete signals are provided. These discrete signals may also be assigned as input and output triggers and discrete channels 7-12 may be used as an external source for remote terminal hardwired addressing when enabled. The input threshold for the discretes is +2.7 V on the RAR15XF.

Output specs:
- Open drain output with Vds = 43 V max.
- Vol = 0.35 V max @ Iol = 500 mA.

Input specs:
- Input interally pulled to 3.3V via 10 KΩ after input protection diode.
- Input range -0.5 to 43 V max
- Vil = -0.5 V to 2.0 V
- Vih = 2.4 V to 43 V.

18.9 Differential I/O

A differential clock input and a differential time-tag reset input is provided. The differential clock input accepts a 1 MHz – 10 MHz external clock input (under software control). The reset input resets the card's time tag to zero upon receipt of a valid (greater than 50 ns positive pulse) input signal. The inputs are compatible with TIA/EIA-485-A specifications. They can be used single-ended as well since the negative terminal is biased at ~ 1.9V.

Output specs:
- Vod (differential) = 2 V min into 50 Ω load, 3.3 V max.

Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 125 uA max @ Vin = 12 V, -100 uA max @ Vin = -7 V
Rin = 96 KΩ min not taking into account Vneg_bias resistors.

Negative pin bias:

Vneg_bias = ~1.9 V via 10 KΩ pull-up to 3.3V and 13.7 KΩ pull-down to ground.

18.10 Hardwired RT Address

For 1553 channel 1, its External RT Addressing is traded for discretes 7-12. The remaining 1553 channels RT Address can be configured in Flash.

18.11 Flash Configurable 1553 Options

The RAR15XMC-FIO has 1553 channel options that may be individually configured by the user on a per-channel basis using the Abaco Flash Configurable Programmer Windows utility.

Table 18-5 Flash Configurable 1553 Options

Channel Option	Description	Default
RT Offset Value	Valid entries are 0-31	0
1760 Startup	Enables or disables 1760 response	Disabled
HWRT Mode	RT Address = Offset or Offset + Hardwire RT address	Offset + Hardwire RT Address
Enforce BM Only	When enabled will not permit BC or RT operation.	Disabled
Startup Coupling	Selects 1553 bus coupling desired at powerup on boards with coupling relays (standard). Factory default is transformer coupling.	Transformer
A/B Startup	Selects Mil-STD-1553A or B protocol	1553B
Single Validated RT	When SRT is selected the channel functions as a single validated RT and as a BM. In Standard Mode the board has Dual or Multi-function, depending on what was purchased.	Standard

18.12 Memory

The RAR15XMC-FIO requires a 16-MByte address block. The BIOS maps the board into memory space at an address above the total amount of RAM in the computer.

The board has 8 MBytes of volatile RAM (GSI P/N GSI8642Z36GB-250M) and 32 or 64 Mbit of non-volatile flash memory (Winbond P/N W25Q32BVSSAG or W25Q32BVSSAG (supply dependent) used for board and FPGA configuration. This non-volatile flash memory is not accessible for general purpose use and is only accessible through the Abaco Flash Configurable Programmer software utility.

Flash memory can be write protected in either of two ways, in-system or flash based:

- **In System**: The active high assertion of the XMC MVMRO write prohibit signal on the P15 connector prevents flash from being written to in-system however, if the MVMRO is un-asserted or the board placed in another system where the MVMRO signal is not asserted flash may once again be written to.
- **Flash Based:** The flash based method requires enabling the Write Protect Board Option through the Abaco Flash Configurable Programmer Windows utility. Once this bit in enabled and board power is cycled the flash cannot be written to again without being returned to the factory for reprogramming.

18.13 Mechanical and Power

- Weight: 101 grams or 3.54 oz. (RAR15XMC-FIO-1084n, non-coated)
- Size: Single-width XMC mezzanine card conforming to the standard IEEE 1386-2001 form factor (143.75 mm x 74 mm)
- Power (Supplied through the XMC P15 VPWR pins): +5 V or +12 V
- Power (All channels terminated and transmitting at 25% duty cycle): 4.5 W (VPWR= +5 V)

19 • R15-MPCIE Installation

19.1 R15-MPCIE Installation Procedure

19.1.1 Hardware Installation

1. Remove the board from the anti-static bubble pack and lay the board on top of the bag. This prevents static discharge from damaging the board when the chassis is opened.
2. Connect a transition cable assembly to the board to make the required MIL-STD-1553 bus and various I/O connections.
3. Insert the R15-MPCIE into the Mini-PCIe slot.

19.2 R15-MPCIE Board Layout

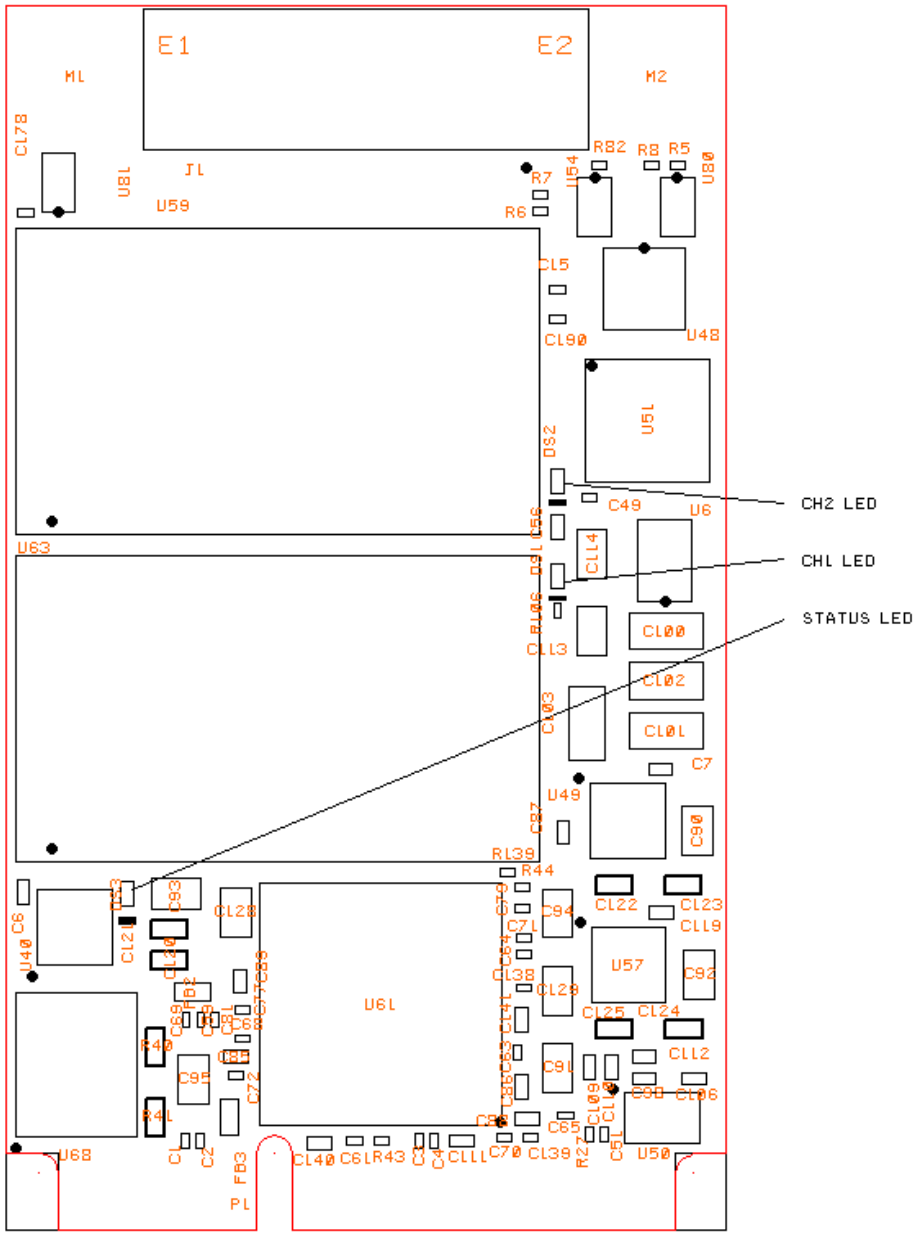
Figure 19-1 R15-MPCIE

19.3 Status LEDs

There are three LEDs on the R15-MPCIE as shown in Figure 20-2.

- **CH 1, CH 2 – 1553 Bus Activity -** The status LED for each 1553 channel illuminates when 1553 bus traffic is active.
- **Status** – This LED is solid green when the FPGA is not programmed, turns off when a successful FPGA configuration has loaded and flashes under normal conditions when the PCIe link is active.

Figure 19-2 R15-MPCIE LED Location



19.4 R15-MPCIE I/O Connectors

The R15-MPCIE has two I/O connectors: a standard 50-pin SlimStack 0.4mm pitch flexible cable connector (Molex part number 503304-5040/503304-5042) on the back side of the board which is always present, and, an optional top side 37-pin rugged nano-D connector (Omnetics RoHS PN A39100-837, identical to non-RoHS PN A29100-037) shown in Figure 19-1.

The Molex mating connector is Molex part number 503308-5010/503308-5012 and the Omnetics mating connector with 18" 30 AWG leads and retaining screws is Omnetics part number A28000-037.

19.4.1 R15-MPCIE I/O Connector Pin Assignments

Table 19-1 R15-MPCIE 37-pin Nano-D (J1) Pin Assignments

Pin	Function	Pin	Function
1	IRIG_IN+	20	IRIG_IN-
2	IRIG_OUT	21	485_NEG1
3	485_POS1	22	GND
4	GND	23	/USER_LED2
5	/USER_LED1	24	JTAG_TDO
6	JTAG_TDI	25	GND
7	JTAG_TMS	26	+3.3V
8	+2.5V	27	GND
9	JTAG_TCK	28	ADISC 2
10	ADISC 1	29	GND
11	GND	30	RTADP
12	RTAD2	31	RTAD4
13	RTAD1	32	RTAD3
14	RTAD0	33	1553_CH2B+
15	1553_CH2B-	34	1553_CH2A+
16	1553_CH2A-	35	Chassis*
17	Chassis	36	1553_CH1B+-
18	1553_CH1B-	37	1553_CH1A+
19	1553_CH1A-		

NOTE

The Chassis connections are tied to the board mounting holes and are intended to be used as the MIL-STD-1553 shields.

Table 19-2 R15-MPCIE 50-pin Molex (J2) Pin Assignments

Pin	Function	Pin	Function
1	IRIG_OUT	26	IRIG_IN+
2	485_POS1	27	IRIG_IN-
3	485_NEG1	28	GND
4	USER_LED2	29	USER_LED1
5	+3.3V	30	+2.5V
6	JTAG_TDO	31	JTAG_TDI
7	JTAG_TMS	32	GND
8	JTAG_TCK	33	GND
9	n/c	34	n/c
10	GND	35	GND
11	GND	36	GND
12	ADISC 2	37	ADISC 1
13	RTADP	38	RTAD2
14	RTAD4	39	RTAD1
15	RTAD3	40	RTAD0
16	Chassis	41	Chassis
17	Chassis	42	Chassis
18	1553_CH2B+	43	1553_CH2B-
19	1553_CH2B+	44	1553_CH2B-
20	1553_CH2A+	45	1553_CH2A-
21	1553_CH2A+	46	1553_CH2A-
22	1553_CH1B+	47	1553_CH1B-
23	1553_CH1B+	48	1553_CH1B-
24	1553_CH1A+	49	1553_CH1A-
25	1553_CH1A+	50	1553_CH1A-

NOTE

The Chassis connections are tied to the board mounting holes and are intended to be used as the MIL-STD-1553 shields.

19.4.2 R15-MPCIE Transition Cable

A Transition Cable is not provided with the R15-MPCIE. There are a variety of options available in Appendix A, Table A-1, under the R15-MPCIE card.

19.5 IRIG Signaling

IRIG input and output signals are provided. Software-selectable internal wrap.

IRIG-B receiver (AM or TTL/DC)
Virig_in: ±5V max
Virig_return: ±5V max. Ground for single-ended IRIG input.
Zin for each input = 22.1 kΩ.

IRIG-B generator (TTL/DC)
Voh_max = 3.47 V - Zout drop
Voh_min = 2.3 V min - Zout drop
Vol = 0.3 V max + Zout drop
Iol / Ioh = 12 mA max
Zout = 100 Ω output series resistance.

19.6 Avionics Discrete I/O

The R15-MPCIE has two discrete I/O signals (ADISC X) available.

Output specs:
Open drain output with Vds = 60 V max.
Vol = 0.4 V max @ Iol = 150 mA

Input specs:
Input interally pulled to 3.3V via 11.5 KΩ after input protection diode.
Input range -0.5 to 60 V max
Vil = -0.5 V to 1.9 V
Vih = 2.1 V to 60 V

19.7 External RT Address

The R15-MPCIE provides Hardwired RT Addressing through dedicated pins. Flash based RT addressing is also available. The input specification is the same as for the

Input specs:
Same as for Avionics Discretes

19.8 Differential I/O

One differential I/O with software-switchable 120-Ω termination resistor is provided. It can be used single-ended as well since the negative terminal is biased at ~ 1.8V.

Output specs:
Vod (differential) = 2 V min into 50 Ω load, 3.3 V max.
Voc (common mode) = 3 V max.

Input specs:

Vth (diff threshold) = ±0.2 V max. with –7 V ≤ Vcm ≤ 12 V
Iin = 125 uA max @ Vin = 12 V, -100 uA max @ Vin = -7 V
Rin = 96 KΩ min not taking into account Vneg_bias resistors.

Negative pin bias:

Vneg_bias = ~1.8 V via 22.1 KΩ series resistor to 1.8 V.

19.9 User LED Outputs

Two open-drain 1553 activity outputs, suitable for driving LEDs, are provided. These can also be used as general purpose Avionics outputs.

Output specs:

Same as for Avionics Discretes

20 • Interface Signals

Each of the boards listed on the front cover provides one or more dual-redundant MIL-STD-1553 interface channels. Other board features can include discretes, differentials, PIOs, triggers, IRIG, 1553 LRU Bus and/or Test Bus and hardwired RT addressing.

With the release of version 6 (aka UCA32) firmware, significant enhancements over V4/V5 UCA (legacy) firmware have been made. It is not available for all products. Table 1-3 “Notes and V6 Firmware Availability” identifies which boards can have V6 firmware. After hardware installation, reading the boards’ CSC Control Register will identify if the board has V6 firmware and reading the LPU Version will identify the exact revision of firmware. Using V6 firmware requires using BusTools/1553-API version 8.x. There is an application note, “AN 020 Transitioning to UCA32 Firmware”, designed to help those that need to convert to the V6 firmware.

This chapter attempts to give a general understanding of the various interface signals and how they may differ between different versions of firmware. However, for an in-depth understanding of V6 firmware, please reference the UCA32 Global Register Reference Manual and the UCA32 LPU Reference Manual. For versions prior to V6, please reference the Mil-Std_1553 UCA Reference Manual.

20.1 MIL-STD-1553 Bus

20.1.1 Overview

A single MIL-STD-1553 interface consists of dual redundant buses. It consists of a primary bus called Bus A and a secondary bus called Bus B. In this manual, each dual redundant 1553 interface is typically referred to as a channel, such as Channel 1, Channel 2, etc. It may also be referred to as a terminal.

Operational modes for a MIL-STD-1553 interface can include a Bus Controller, a Bus Monitor or up to 31 Remote Terminals. Boards in this manual support these modes. However, depending on the board, its firmware version and purchased option, all modes may not be available at the same time. Options may include single-function, dual-function and multi-function configurations.

Single-function boards allow operation in only one of the three 1553 modes at a time: Bus Controller, Bus Monitor or Remote Terminal (up to 31 RTs). Although all three modes are available, the board can operate only in one mode at any given time.

Dual function boards are available on firmware versions 4.50 or greater. It allows the application to run Bus Monitoring along with either Bus Controller or Remote Terminal functions.

Multi-function boards allow any combination of the three modes to operate at the same time. This means a multi-function board can simulate a 1553 bus with a Bus Controller, Bus Monitor and up to 31 Remote Terminals currently.

20.1.2 Bus Coupling

MIL-STD-1553B allows two methods of connecting a terminal to the bus.

- Direct coupled, aka short stub
- Transformer coupled, aka long stub

Direct Coupling can be used when the data bus does not exceed one foot. There are 53.6 Ω isolation resistors on the board for direct coupling to the bus.

Transformer coupling is the most common as it provides better noise immunity and isolation over long distances. It requires a bus coupler external to the board (comprised of transformers and resistors) to connect to the bus.

All standard boards support transformer coupling. Some boards also provide for direct coupling. Depending on the board, the transformer and direct coupled signals may go to the I/O connector directly or may be switched thru relays. If relay equipped, the coupling selection can be programmed in flash for automatic selection at powerup and can also be commanded via the host. At the time of ordering, boards with relays may have the relays removed and resistors installed to hard-wire for transformer or direct coupling. Removing the relays makes the card more ruggedized.

20.1.3 Output Voltage Level

Depending on the board, the MIL-STD-1553 output level may be fixed or adjustable on a per-channel basis via the host. Adjustable output levels are strictly for the test environment. The output level can vary from the standard fixed output level down to zero output in 255 step increments. As a special order, boards that support adjustable output levels may have this feature disabled via hardware.

20.1.4 Bus Connections

Each redundant bus is comprised of differential signals A+ and A- for Bus A and B+ and B- for Bus B. Shield pins are also provided on the connector as the cable coming to our card should be twisted shielded pair. On most of the cards, the SHIELD connections are all tied together and to chassis if one is available. On some older cards, the shields for the individual busses were tied to the transformer secondary center tap as indicated in this manual. This may cause problems meeting the Common Mode Rejection requirement. When using these boards, it may be best to connected all the shields for the various channel cables together at our board end but not connect them to the SHIELD pin(s) on the connector.

Labeling on the I/O connector for Bus A will be something similar to “1553 CH1A+” and “1553 CH1A-”. The SHIELD signal may be associated with a particular 1553 channel or may be stand-alone.

For information on how to connect our cards to a 1553 bus, reference the “Abaco MIL-STD-1553 Tutorial”.

20.1.5 Bus Definitions and Characteristics

MIL-STD-1553 has an older “A” version and the more popular and newer “B” version. Boards in this manual support both formats and each individual channel may be configured in flash to boot up supporting either version. In addition, software can override the powerup configuration and individual RTs may be configured to support either version.

For information regarding MIL-STD-1553, the following are good sources of information:

- Abaco MIL-STD-1553 Tutorial – Provides a basic understanding of 1553
- MIL-STD-1553B – Department of Defense Data Bus specification
- MIL-HDBK-1553A – Users guide for 1553. It also describes the differences between
  MIL-STD-1553A and MIL-STD-1553B
- SAE AS411 – RT Validation test plan

20.2 Avionic Discretes

Many boards listed in this manual feature a number of bi-directional Avionic Discrete signals to be used as general purpose I/O. They are implemented as a low-side switch combined with an input comparator.

The low-side switch is comprised of a FET which in most cases is capable of sinking 0.5 A to ground when the switch is commanded on. When the switch is on, the discrete output pin is driven low. When the switch is off, the output pin is pulled high with a resistor / diode combination to 3.3 V. A comparator provides status of the discretes I/O pin at all times. If the discrete I/O pin needs to be an input, the switch is simply commanded off. The comparator is protected by the previously mentioned diode such that inputs of 40 V will not damage the comparator.

In some cases, as described below, discretes may be traded to be used as triggers and/or External RT Addresses instead of general purpose I/O.

On the I/O connector, they will be labeled something similar to ADISC1, ADISC2, etc. unless they are shared with an External RT Address in which case they will be labeled RTADDR1_0/ADISC1, RTADDR2_0/ADISC2, etc.

20.3 PIOs

Some boards provide for general purpose parallel I/O (PIO). Each of the signals can be individually programmed as an input or output. Note that these I/O are controlled serially and as such, delays of up to 16 µs encountered (between an instruction issued by the host and its effect seen at the targeted I/O)

On the RXMC-1553 product there is an additional delay of up to 16 µs encountered (between an instruction issued by the host and its effect seen at the targeted I/O) due to the serial I/O expanders used to implement ports for avionic discretes and general purpose PIOs. If I/O is interconnected (i.e. PIO bits 5 & 6 are wired together), care should be taken to avoid inadvertently configuring both connected bits as outputs in light of this delay

20.4 Differentials

Some boards have RS485 transceiver(s) capable of being used as general purpose differential input, differential outputs or both.

In some cases, as described below, Differentials may be used as triggers.

20.5 Triggers

There are a variety of triggering possibilities among the different boards. Firmware version also plays a big part in triggering capabilities. Input triggers can be for starting the BC, RT or BM functions as well as loading the time-tag counter. Output triggers can provide a BM trigger or RT synchronization mode code output.

Some boards have a dedicated input and/or output triggers per 1553 channel. Many boards with firmware prior to V6 only supported discrete 7, 8 and 485 channels as input or output triggers. For boards without dedicated trigger I/O and with V6 firmware, any available discrete or differential can be programmed as an input or output trigger.

Trigger inputs and outputs using Avionics Discretes are low true. That is, a transition from high to low defines the trigger. If differentials or dedicated triggers are used, they are high true such that a low to high defines the trigger. The R15-LPCIE is an exception where the dedicated output triggers are low true. Output triggers are a pulse which is active for approximately 50 µs. Input triggers should have a minimum pulse width of 400 ns.

20.6 Test Bus

A Test Bus if so equipped provides a means via relays to switch the 1553 outputs from the I/O connector to an on-card 1553 data bus. There are both A & B busses which are correctly terminated to allow for on-board testing.

20.7 LRU Bus

An LRU Bus contains a Test Bus and the equivalent of a Bus Coupler for each bus brought out to the I/O connector. This allows inputs from an LRU to be tested or perform testing with the selected on-board 1553 channels.

20.8 Hardwired RT Address

20.8.1 Overview

Many boards provide for hardwired RT addressing. When enabled, hardwired RT addressing allows the RT to respond within 150 ms of powerup with the Busy Bit set to messages addressed to it as described in MIL-STD-1760D.

Hardwired RT addressing, if available, is offered in a variety of ways depending on the board and its firmware version. Below are the various Hardwired RT addressing implementations:

- Provided by shared Avionics Discretes
- Provided by dedicated inputs
- Defined solely in flash by the user on a per-channel basis
- Defined by the sum of an external address and a flash based offset provided by the user on a per-channel basis

External RT addressing is provided by shared Avionics Discretes or dedicated inputs and consist of 5 address lines and a parity bit for each available External RT Address. On the I/O connector, a shared pin for External RT Address 1, bit 1 will be RTADDR1_0/ADISC1 and the parity bit will be RTADDR1_P/ ADISC6. For the External RT Address to be valid, the 5 address lines and the parity bit must have odd parity. That is, the total of the 6 inputs that read logic one must be an odd number. External RT addressing input polarity is active high. Onboard pull-ups assure that floating inputs are read as logic one and grounded inputs are read as logic zero.

With a valid hardwired RT address, the RT continues to respond with the busy bit until the host initializes an RT(s) and sets the RT run bit. Using hardwired RT addressing does not limit the function of the board The Bus Controller and Bus Monitor (if available) can still be used.

20.8.2 Boards without Flash Based RT Addressing

Avionics Discretes Shared with External RT Addressing

For boards that share Avionics Discretes with External RT Address, there is a pin on the connector or jumper on the card with a label similar to ~HWRT_EN. When this line is pulled low, it forces all dual function External RT Address bit / Avionics Discrete pins to be External RT Address pins.

As defined for the particular boards in this manual, if there is only 1 set of External RT Address pins, then they apply to only 1553 channel 1. That is, only channel 1 responds with busy. If there are 2 sets of External RT Address pins, then they apply to 1553 channels 1 & 2 only, and so forth. Remember that the External RT Address must have correct parity for the particular channel to respond with busy. If the board has 2 sets of External RT Addresses, and a busy response is only desired from channel 1, channel 2 External RT Addresses can simply be unconnected. This causes bad parity on channel 2, and it will not respond with busy.

Dedicated External RT Addressing Inputs

For boards with dedicated external RT addressing, setting an RT Address with correct parity causes the particular 1553 channel to respond with busy.

20.8.3 Boards with Flash Based RT Addressing

For boards that have flash-based RT Addressing, there are a variety of options. Using the Abaco Flash Configurable Programmer, an RT Address can be defined in flash for each channel so that each channel can respond with busy if desired. A per-channel address can also be defined by using the External RT Address (if available) for channel 1 (only) and adding to that an arbitrary offset for any of the available channels. Additionally, respond with busy can be disabled on a per-channel basis.

If the board has shared External RT Addressing and if the ~HWRT_EN pin is pulled low, the board behaves as if there were no flash based addressing.

The table below shows the various options of using flash based RT Addressing with External Hardwired RT Addressing.

Table 20-1 1760 Start-Up Options

Board Pin	Flash Programmer Selection Modes		Ext RT Addr Parity	RT Address used for 1760
~HWRT EN	HWRT Mode	1760 Startup		
1	Offset + HWRT Addr	Enable	Good	CH1 = CH1 Offset + CH1 Ext RT Addr CH2 = CH2 Offset + CH1 Ext RT Addr CH3 = CH3 Offset + CH1 Ext RT Addr CH4 = CH4 Offset + CH1 Ext RT Addr
1	Offset + HWRT Addr	Enable	Bad	No 1760 startup due to bad parity
1	Offset	Enable	X	CH1 = CH1 Offset CH2 = CH2 Offset CH3 = CH3 Offset CH4 = CH4 Offset
1	X	Disable	X	No 1760 startup
0	X	X	Good	CH1 = Disc [6:1] CH2 = Disc [14:9] if available
0	X	X	Bad	No 1760 startup due to bad parity
X = Don't Care				

20.9 Flash Configurable 1553 Options

Most boards have 1553 channel options that may be individually configured by the user on a per-channel basis using the Abaco Flash Configurable Programmer Windows utility. All firmware loaded from flash memory with an LPU revision of at least 6.00 have flash configurable 1553 options. Earlier firmware on selected platforms also has flash configurable 1553 options.

Table 20-2 Flash Configurable 1553 Options

Channel Option	Description	Default
RT Offset Value	Valid entries are 0-31	0
1760 Startup	Enables or disables MIL-STD-1760 startup RT response	Disabled
HWRT Mode	RT Address = Offset or Offset + Hardwire RT address	Offset + Hardwire RT Address
Enforce BM Only	When enabled will not permit BC or RT operation.	Disabled
Startup Coupling	Selects initial 1553 bus coupling.	Transformer
A/B Startup	Selects Mil-STD-1553A or B protocol	1553B
Single Validated RT	When SRT is selected, the channel functions as a single validated RT and as a BM. In Standard Mode, the board has Dual or Multi-function, depending on what was purchased.	Standard

This non-volatile flash memory is not accessible for general purpose use and is only accessible through the Abaco Flash Configurable Programmer software utility.

Flash memory can be write-protected in either of two ways, in-system or flash based:

- **Flash Based:** The flash based method requires enabling the Write Protect Board Option through the Abaco Flash Configurable Programmer Windows utility. Once this bit in enabled and board power is cycled, the flash cannot be written to again without being returned to the factory for reprogramming.
- **In-System**: On some boards, a connector pin is provided to enable/disable flash write protection.

20.10 IRIG Signaling

Most boards have IRIG-B capability. IRIG time may be received on the signals IRIG IN and IRIG IN Return. The following IRIG formats are accepted:

Table 20-3 IRIG Format

Format	Modulation Frequency	Frequency/ Resolution	Coded Expressions
B	0, 1	0, 2	0, 1, 2, 3

When enabled by the software and if available, IRIG OUT will transmit IRIG B002 data from the onboard IRIG encoder.

A • Appendix – Transition Cables

Cables that connect to our boards are called transition cables. Some are provide with the card and others must be ordered separately. Some transition cables are shared among different products and some cards require multiple cables. The table below provides a cross reference to indicate what transition cable(s) are required with a particular board and if they are included or not with the card. Each of the following sections details each of the available transition cables available for the boards identified in this manual.

For the latest details on Abaco-supplied cabling, consult the Online Cabling Guide available on Abaco's website.

LINK
https://www.abaco.com

Table A-1 Board / Transition Cable Cross Reference

Card	Platform	Cable Name	Cable PN	Comments
AMC-1553	AMC	N/A	N/A	Contact Abaco Sales regarding availability.
Q104-1553	PC/104	Q104-1553 Mating connector Mounting Kit	2220-007	One mating connector included with card.
QCP-1553	CPCI	RCONQPMC-X	1320-028-8 (X=1) 1320-020-8 (X=2) 1320-021-8 (X=4)	One each included with each one, two or four channel card where X = 1, 2 or 4.
QPCX-1553	PCI	RCONQPMC-X	1320-028-8 (X=1) 1320-020-8 (X=2) 1320-021-8 (X=4)	One each included with each one, two or four channel card where X = 1, 2 or 4.
QPM-1553	PMC	RCONQPMC-X	1320-028-8 (X=1) 1320-020-8 (X=2) 1320-021-8 (X=4)	One each included with each one, two or four channel card where X = 1, 2 or 4.
QVXI2-1553X	VME	RCONP1553-1	1320-019-8	One included per each 1553 channel with card (non-IRIG).
QVXI2-1553X w/IRIG	VME	CONW1553-1	1320-036	One included with card for each 1553 channel.
R15-AMC	AMC	R15-AMC Transition Cable	1320-069-9	One four channel cable included with each card.
R15-EC	Express Card	RCONR15-EC-X	1320-060-8 (X=1) 1320-061-8 (X=2)	One each included with each one or two channel card where X = 1 or 2.
R15-LPCIE	Low Profile PCIE	RCONR15-LPCIE-X	1320-076-8 (X=1) 1320-077-8 (X=2)	Not included with card. Use suffix "–CBL" to include with one or two channel configurations where X = 1 or 2.
R15-MPCIE	Mini PCIE	RCONR15MPCIE	1320-105-8	Slim-stack connector via flex print to SCSI-50. Not included with card.
		RCONR15MPCIER	1320-102-8	Rugged connector to SCSI-50 panel mount. Not included with card.

Card	Platform	Cable Name	Cable PN	Comments
		RCONR15MPCIE-X	1320-105-8 and 1320-076-8 (X=1) or 1320-077-8 (X=2)	RCONR15MPCIE-X = RCONR15MPCIE + RCONR15-LPCIE-X where X = 1 or 2. Not included with card.
		RCONR15MPCIER-X	1320-102-8 and 1320-076-8 (X=1) or 1320-077-8 (X=2)	RCONR15MPCIER-X = RCONR15MPCIER + RCONR15-LPCIE-X where X = 1 or 2. Not included with card.
		RCONMPCIER	1320-104-8	Rugged 37 position connector with custom thrumbscrews and 18" flying leads. Not included with card.
		OMNETICS A28000-037	N/A	Rugged 37 position connector with standard jack screws and 18" flying lead. Not included with card.
R15-USB	USB	N/A	N/A	None Available
RAR15XF	XMC	RCONRAR15-X	1320-083-8 (X=2) 1320-084-8 (X=4)	Not included with card. Use suffix "–CBL" to include with two or four channel configurations where X = 2 or 4.
RPCC-D1553	PCMCIA	RCONPCCD-X	1320-089-8 (X=1) 1320-088-8 (X=2)	One each included with each one or two channel card where X = 1 or 2.
RPCIE-1553	PCIE	RCONQPMC-X	1320-028-8 (X=1) 1320-020-8 (X=2) 1320-021-8 (X=4)	One each included with each one, two or four channel card where X = 1, 2 or 4.
RQVME2-1553	VME	RCONP1553-1	1320-019-8	One included with card for each 1553 channel.
RQVME2-1553 w/IRIG	VME	CONW1553-1	1320-036	One included with card for each 1553 channel.
RXMC1553	XMC	RCONQPMC-X	1320-028-8 (X=1) 1320-020-8 (X=2)	One each included with each one or two channel card where X = 1 or 2.
RXMC2-1553	XMC	RCONRXMC2-X	1320-081-8 (X=2) 1320-075-8 (X=4)	Not included with card. Use suffix "–CBL" to include with two or four channel configurations where X = 2 or 4.

A.1 RCONQPMC-X Transition Cable

A.1.1 Cable Description

The cable transitions from a SCSI-68 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and one D-Sub female 50 pin connector for additional I/O. A list of the cable components is shown in the table below. This cable is available in one, two or four channel versions where X = 1, 2 or 4 after the dash in the product name of this Appendix section. Pictures of the cables are shown in the figures below. The nominal cable length from the back of the SCSI-68 to the backs of the Twinax connectors is 10". The nominal cable length from the back of the SCSI-68 to the back of the D-Sub 50 is 8".

Table A-2 Transition Cable Components

Connector	Description
SCSI-68	TE 1-5750913-7 or equiv
D-Sub 50 pin	Amphenol L77DD50S or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-1 RCONQPMC-1

Figure A-2 RCONQPMC-2

Figure A-3 RCONQPMC-4

A.1.2 Transition Cable Pinouts

The tables below provides pin assignments for the 1553 Twinax and D-Sub 50 pin connectors. Since the RCONQPMC connector is used on multiple products, the D-Sub signals can take on different assignements. Therefore, pinouts for the D-Sub are provided for each product where it is used.

The D-Sub is J3 for one-channel cable assemblies and J5 for two and four-channel cable assemblies.

Table A-3 One-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B

Table A-4 Two-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B

Table A-5 Four-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B
J6	Channel 3, Bus A
J7	Channel 3, Bus B
J8	Channel 4, Bus A
J9	Channel 4, Bus B

Table A-6 D-Sub for the QPCI-1553 / QPCX-1553

Pin	Signal	Pin	Signal
1	RTADD1_0/ADSIC 1	26	GND
2	RTADD1_1/ADSIC 2	27	-
3	GND	28	GND
4	RTADD1_2/ADSIC 3	29	LRUA Shield (See Note)
5	RTADD1_3/ADSIC 4	30	-
6	GND	31	-
7	RTADD1_4/ADSIC 5	32	-
8	RTADD1_P/ADSIC 6	33	-
9	ADSIC 7	34	485/422 CH1+
10	ADSIC 8	35	485/422 CH1-
11	ADSIC 9	36	485 Shield
12	GND	37	LRUA+
13	EXT CLK+/Trigger+	38	LRUA -

Pin	Signal
14	EXT CLK-/Trigger-
15	-
16	GND
17	-
18	ADSIC 10
19	GND
20	GND
21	GND
22	-
23	-
24	-
25	GND

Pin	Signal
39	GND
40	LRUB+
41	LRUB -
42	LRUB Shield (See Note)
43	-
44	-
45	GND
46	IRIGB IN
47	IRIGB OUT
48	IRIGB IN Return
49	-
50	GND (cable shield)

NOTE

For the QPCI, the LRUx Shield signals are tied to their respective transformer secondary center taps. On the QPCX, these signals do not exist and are open.

Table A-7 D-Sub for the QPM/QPMC and the QPM -H

Pin	QPM/QPMC Signal	QPM-H Signal
1	RTADDR1_0/ ADSIC 1	RTADDR1_0/ ADSIC 1
2	RTADDR1_1/ ADSIC 2	RTADDR1_1/ ADSIC 2
3	GND	GND
4	RTADDR1_2/ ADSIC 3	RTADDR1_2/ ADSIC 3
5	RTADDR1_3/ ADSIC 4	RTADDR1_3/ ADSIC 4
6	GND	GND
7	RTADDR1_4/ ADSIC 5	RTADDR1_4/ ADSIC 5
8	RTADDR1_P/ ADSIC 6	RTADDR1_P/ ADSIC 6
9	ADSIC 7	ADSIC 7/TRIG0
10	ADSIC 8	ADSIC 8/TRIG1
11	RTADDR2_0/ ADSIC 9	RTADDR2_0/ ADSIC 9
12	GND	GND
13	EXT IN+	EXT IN+
14	EXT IN -	EXT IN -
15	~HWRT_EN	~HWRT_EN
16	GND	GND
17	-	-
18	RTADD2_1/ ADSIC 10	RTADD2_1/ ADSIC 10
19	RTADD2_2/ ADSIC 11	485_5+

Pin	QPM/QPMC Signal	QPM-H Signal
26	ADSIC 16	485_7-
27	ADSIC 17	485_8+
28	ADSIC 18	485_8-
29	GND	GND
30	-	-
31	-	-
32	-	-
33	-	-
34	-	485_1+
35	-	485_1-
36	GND	GND
37	-	485_2+
38	-	485_2-
39	GND	GND
40	-	485_3+
41	-	485_3-
42	GND	GND
43	-	485_4+
44	-	485_4-

Pin	QPM/QPMC Signal	QPM-H Signal
20	RTADD2_3/ ADSIC 12	485_5-
21	GND	GND
22	RTADD2_4/ ADSIC 13	485_6+
23	RTADD2_P/ ADSIC 14	485_6-
24	ADSIC 15	485_7+
25	GND	GND

Pin	QPM/QPMC Signal	QPM-H Signal
45	GND	GND
46	IRIGB IN	IRIGB IN
47	IRIGB OUT	IRIGB OUT
48	IRIGB IN Return	IRIGB IN Return
49	-	-
50	GND (cable shield)	GND (cable shield)

NOTE

For the QPMC, all of the transformer secondary center taps are tied together and become the signal 1553_Shield. For the QPM, the transformer secondary center taps are not connected. The signal 1553_Shield is tied to the mounting bossess.

Table A-8 D-Sub for the QCP-1553

Pin	Signal
1	RTADD1_0/ADSIC 1
2	RTADD1_1/ADSIC 2
3	GND (for ADISC1)
4	RTADD1_2/ADSIC 3
5	RTADD1_3/ADSIC 4
6	GND (for ADISC2)
7	RTADD1_4/ADSIC 5
8	RTADD1_P/ADSIC 6
9	ADSIC 7
10	ADSIC 8
11	RTADDR2_0/ADSIC 9
12	GND
13	485+ IN
14	485- IN
15	~HW_RT_EN
16	GND
17	-
18	RTADDR2_1/ADSIC 10
19	RTADDR2_2/ADSIC11
20	RTADDR2_3/ADSIC11
21	GND
22	RTADDR2_4/ADSIC13

Pin	Signal
26	ADSIC16
27	ADSIC17
28	ADISC18
29	GND
30	-
31	-
32	-
33	-
34	485+ OUT
35	485- OUT
36	GND
37	-
38	-
39	GND
40	-
41	-
42	GND
43	-
44	-
45	GND
46	IRIGB IN
47	IRIGB OUT

Pin	Signal
23	RTADDR2_P/ADSIC14
24	ADSIC15
25	GND

Pin	Signal
48	IRIGB GND
49	-
50	GND (cable shield)

Table A-9 D-Sub for the RPCIE-1553

Pin	Signal
1	RTADD1_0/ADISC 1
2	RTADD1_1/ADISC 2
3	GND
4	RTADD1_2/ADISC 3
5	RTADD1_3/ADISC 4
6	GND
7	RTADD1_4/ADISC 5
8	RTADD1_P/ADISC 6
9	ADSIC 7
10	ADSIC 8
11	ADSIC 9
12	GND
13	EXT CLK+/Trigger+
14	EXT CLK-/Trigger-
15	~HWRT_EN
16	GND
17	
18	ADISC 10
19	ADISC11/RTADD2_2
20	ADISC12/RTADD2_3
21	GND
22	ADISC13/RTADD2_4
23	ADISC14/RTADD2_P
24	ADISC15
25	GND

Pin	Signal
26	ADISC16
27	ADISC17
28	ADISC18
29	GND
30	
31	
32	
33	
34	
35	
36	GND
37	
38	
39	GND
40	
41	
42	GND
43	
44	
45	GND
46	IRIGB IN
47	IRIGB OUT
48	IRIGB IN Return
49	
50	GND (cable shield)

Table A-10 D-Sub for the RXMC-1553

Pin	Signal
1	RTADDR1_0
2	RTADDR1_1
3	GND
4	RTADDR1_2
5	RTADDR1_3
6	GND
7	RTADDR1_4
8	RTADDR1_P
9	CH1 EXTTRIG
10	CH2 EXTTRIG
11	RTADDR2_0
12	GND
13	RTN_DISCRETE2
14	RTN_DISCRETE3
15	
16	GND
17	
18	RTADD2_1
19	RTADD2_2
20	RTADD2_3
21	RTN_DISCRETE4
22	RTADD2_4
23	RTADD2_P
24	28V_DISCRETE1
25	GND

Pin	Signal
26	28V_DISCRETE2
27	28V_DISCRETE3
28	28V_DISCRETE4
29	GND
30	
31	
32	
33	
34	PIO0 EIA0N_DISC5
35	PIO1 EIA0P_DISC6
36	RTN_DISCRETE1
37	PIO2_EIA1N_DISC7
38	PIO3_EIA1P_DISC8
39	GND
40	PIO4_EIA2N_DISC9
41	PIO5_EIA2P_DISC10
42	GND
43	PIO6_EIA3N_DISC11
44	PIO7_EIA3P_DISC12
45	GND
46	IRIGB IN
47	IRIGB OUT
48	IRIGB IN Return
49	
50	GND (cable shield)

A.2 RCONP1553-1 Transition Cable

A.2.1 Cable Description

The cable transitions from a DB15 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for a 1553 channel and two male BNC jacks for triggers. A list of the cable components is shown in the table below. A picture of the cable is shown in the figure below. The nominal cable length from the back of the DB15 to the backs of the BNC and Twinax connectors is 6″.

Table A-11 Transition Cable Components

Connector	Description
DB15	TE 5-747908-2 or equiv
BNC	Trompeter CJ20-5 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-4 RCONP1553-1

A.2.2 Transition Cable Pinouts

The table below provides pin assignments for the 1553 Twinax and Trigger Coax connectors.

Table A-12 Twinax & Coax Connectors

Connector	Signal
A	1553, Bus A
B	1553, Bus B
EXTIN	Ext Trigger In
EXTOUT	Ext Trigger Out

A.3 CONW1553-1 Transition Cable

A.3.1 Cable Description

The cable transitions from a DB15 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for a 1553 channel and four male BNC jacks for triggers and IRIG. A list of the cable components is shown in the table below. A picture of the cable is shown in the figure below. The nominal cable length from the back of the DB15 to the backs of the BNC and Twinax connectors is 6″.

Table A-13 Transition Cable Components

Connector	Description
DB15	TE 5-747908-2 or equiv
BNC	Trompeter CJ20-5 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-5 CONW1553-1

A.3.2 Transition Cable Pinouts

The table below provides pin assignments for the 1553 Twinax and Trigger and IRIG Coax connectors.

Table A-14 Twinax & Coax Connectors

Connector	Signal
A	1553, Bus A
B	1553, Bus B
EXTIN	Ext Trigger In
EXTOUT	Ext Trigger Out
IRIGIN	irig In
IRIGOUT	IRIG Out

A.4 RCONR15-EC-X Transition Cable

A.4.1 Cable Description

The cable transitions from a Champ 36 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and one D-Sub female 9 pin connector for additional I/O. A list of the cable components is shown in the table below. This cable is available in one or two channel versions where X = 1 or 2 after the dash in the product name of this Appendix section. Pictures of the cables are shown in the figures below. The nominal cable length from the back of the Champ 36 connector to the front of the Twinax connectors is 36″ and the nominal cable length from the back of the Champ 36 to the back of the D-Sub 9 is 4″.

Table A-15 Transition Cable Components

Connector	Description
Champ 36	TE 5175677-5 or equiv
D-Sub 9 pin	Tyco 5-747905-5 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-6 RCONR15-EC-1

Figure A-7 RCONR15-EC-2

A.4.2 Transition Cable Pinouts

The tables below provides pin assignments for the D-Sub 9 pin and 1553 Twinax connectors.

Table A-16 D-Sub 9 Pin Assignments

Pin	Signal
1	IRIGB IN
2	IRIGB_OUT
3	GND
4	TRIG IN
5	TRIG RTN [GND]
6	DISCRETE I/O 1
7	DISCRETE I/O 2
8	GND
9	TRIG OUT

Table A-17 One-channel Twinax Connectors

Connector	Signal
CH1_A	Channel 1, Bus A
CH1_B	Channel 1, Bus B

Table A-18 Two-channel Twinax Connectors

Connector	Signal
CH1_A	Channel 1, Bus A
CH1_B	Channel 1, Bus B
CH2_A	Channel 2, Bus A
CH2_B	Channel 2, Bus B

A.5 RCONR15-LPCIE-X Transition Cable

A.5.1 Cable Description

The cable transitions from a SCSI-50 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and one D-Sub female 37 pin connector for additional I/O. A list of the cable components is shown in the table below. This cable is available in one or two channel versions where X = 1 or 2 after the dash in the product name of this Appendix section. Pictures of the cables are shown in the figures below. The nominal distance from the front of the SCSI-50 to the front of the Twinax connectors is 12″. The nominal distance from the back of the SCSI-50 to the back of the D-Sub 37 is 8″.

Table A-19 Transition Cable Components

Connector	Description
SCSI-50	TE 5749111-4 or equiv
D-Sub 37 pin	TE 5-747917-5 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-8 RCONR15-LPCIE-1

Figure A-9 RCONR15-LPCIE-2

A.5.2 Transition Cable Pinouts

The tables below provides pin assignments for the D-Sub 37 pin and 1553 Twinax connectors.

Table A-20 D-Sub 37 Pin Assignments

Pin	Function	Pin	Function
1	Trig_In_CH1	20	Trig_In_CH2
2	GND	21	GND
3	IRIG_RTN	22	IRIG_Output
4	ADISC12	23	IRIG_In
5	ADISC10	24	ADISC11
6	ADISC8	25	ADISC9
7	GND	26	ADISC7
8	ADISC6	27	GND
9	ADISC5	28	ADISC2
10	ADSIC4	29	ADISC1
11	ADISC3	30	DNG
12	GND	31	RTAD1
13	RTAD0	32	RTAD2
14	RTAD3	33	Trig_Out_CH1
15	RTAD4	34	485_POS1
16	RTADP	35	485_POS2
17	485_NEG1	36	Trig_Out_CH2
18	485_NEG2	37	Unused
19	Unused		

Table A-21 One-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B

Table A-22 Two-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B

A.6 RCONRAR15-X Transition Cable

A.6.1 Cable Description

The cable transitions from a male SCSI-68 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and a second male SCSI-68 pin connector for Arinc and additional I/O. A list of the cable components is shown in the table below. This cable is available in two or four channel versions where X = 2 or 4 after the dash in the product name of this Appendix section. Pictures of the cables are shown in the figures below. The nominal cable length from the back of the boards SCSI-68 mating connector to the backs of the Twinax connectors is 10″. The nominal cable length from the back of the boards SCSI-68 mating connector to the back of the other SCSI-68 connector 58″.

Table A-23 Transition Cable Components

Connector	Description
SCSI-68	TE 1-5750913-7 or equiv (2 pl)
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-10 RCONRAR15-2

Figure A-11 RCONRAR15-4

A.6.2 Transition Cable Pinouts

The tables below provides pin assignments for the SCSI-68 pin and 1553 Twinax connectors.

Table A-24 SCSI-68 Pin Assignments

Pin	Function	Pin	Function
1	1553_CH4B+	35	1553_CH4B-
2	1553_CH4A+	36	1553_CH4A-
3	429_RX1_A	37	429_RX1_B
4	429_RX2_A	38	429_RX2_B
5	429_RX3_A	39	429_RX3_B
6	429_RX4_A	40	429_RX4_B
7	429_RX5_A	41	429_RX5_B
8	429_RX6_A	42	429_RX6_B
9	429_RX7_A	43	429_RX7_B
10	429_RX8_A	44	429_RX8_B
11	1553_CH3B+	45	1553_CH3B-
12	1553_CH3A+	46	1553_CH3A-
13	429_RX9_A/TRIG_IN_CH1	47	429_RX9_B/TRIG_IN_CH2
14	429_RX10_A/TRIG_IN_CH3	48	429_RX10_B/TRIG_IN_CH3
15	GND	49	GND
16	429_RX11_TX1_A	50	429_RX11_TX1_B
17	429_RX12_TX2_A	51	429_RX12_TX2_B
18	429_RX13_TX3_A	52	429_RX13_TX3_B
19	429_RX14_TX4_A	53	429_RX14_TX4_B
20	429_RX15_TX5_A/DIS_1	54	429_RX15_TX5_B/DIS_2
21	429_RX16_TX6_A/DIS_3	55	429_RX16_TX6_B/DIS_4
22	429_RX17_TX7_A/DIS_5	56	429_RX17_TX7_B/DIS_6
23	429_RX18_TX8_A	57	429_RX18_TX8_B
24	IRIG_IN+	58	IRIG_IN-
25	1553_CH2B+	59	1553_CH2B-
26	1553_CH2A+	60	1553_CH2A-
27	IRIG_TX	61	GND
28	EXTCLK+	62	EXTCLK-
29	EXTRST+	63	EXTRST-
30	DISCRETE 7/RTAD0	64	DISCRETE 8/RTAD1
31	DISCRETE 9/RTAD2	65	DISCRETE 10/RTAD3

Pin	Function
32	DISCRETE 11/RTAD4
33	1553_CH1B+
34	1553_CH1A+

Pin	Function
66	DISCRETE 12/RTADPTY
67	1553_CH1B-
68	1553_CH1A-

Table A-25 Two-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B

Table A-26 Four-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B
J5	Channel 3, Bus A
J6	Channel 3, Bus B
J7	Channel 4, Bus A
J8	Channel 4, Bus B

A.7 RCONR15MPCIE Transition Cable

A.7.1 Cable Description

The cable transitions from a Molex slim-stack 50 pin connector to a SCSI-50 female PC panel mount connector providing all the card's I/O. A list of the cable components is shown in the table below. A picture of the cable is shown in the figures below. The SCSI-50 end can be used with the RCONR15-LPCIE-1 and -2 transition cables. The nominal cable length including connectors is 10″, end to end.

Table A-27 Transition Cable Components

Connector	Description
Slim-Stack	Molex 503308-5010/503308-5012
SCSI-50	TE 5787170-5 or equiv

Figure A-12 RCONR15MPCIE

Figure A-13 RCONR15MPCIE Slim-Stack Zoom

Figure A-14 RCONR15MPCIE SCSI Zoom

A.7.2 Transition Cable Pinouts

The table below provides pin assignments for the SCSI-50 connector.

Table A-28 SCSI-50 Connectors

Pin	Function	Pin	Function
1	1553_CH1A-	26	1553_CH1A+
2	NC	27	NC
3	GND	28	GND
4	Chassis*	29	IRIG_OUT
5	IRIG_Return	30	IRIG_IN
6	NC	31	NC
7	1553_CH1B-	32	1553_CH1B+
8	NC	33	NC
9	NC	34	NC
10	GND	35	GND
11	NC	36	NC
12	~USER_LED2	37	~USER_LED1
13	1553_CH2A-	38	1553_CH2A+
14	GND	39	ADISC 2
15	RTAD0	40	ADISC 1
16	Chassis*	41	GND
17	RTAD3	42	RTAD1
18	RTAD4	43	RTAD2
19	1553_CH2B-	44	1553_CH2B+
20	RTADP	45	NC
21	485_NEG1	46	485_POS1
22	NC	47	NC

Pin	Function
23	NC
24	Chassis*
25	NC

Pin	Function
48	NC
49	NC
50	NC

NOTE

The chassis connections are tied to the R15-MPCIE Rugged 37 pin connector shell and board mounting holes and may be used as the MIL-STD-1553 shields.

A.8 RCONR15MPCIER Transition Cable

A.8.1 Cable Description

The cable transitions from a rugged 37 position pin connector to a SCSI-50 female PC panel mount connector providing all the card's I/O. A list of the cable components is shown in the table below. A picture of the cable is shown in the figures below. The SCSI-50 end can be used with the RCONR15-LPCIE-1 and -2 transition cables. The nominal cable length from the back of the Rugged 37 pin connector to the back of the SCSI-50 connector is 8″.

Table A-29 Transition Cable Components

Connector	Description
Rugged 37 pin	RCONMPCIER (custom Omnetics Nano-D 37 pin)
SCSI-50	TE 5787170-5 or equiv

Figure A-15 RCONR15MPCIER

Figure A-16 RCONR15MPCIER Rugged 37 pin Zoom

Figure A-17 RCONR15MPCIER SCSI Zoom

A.8.2 Transition Cable Pinouts

The table below provides pin assignments for the SCSI-50 connector.

Table A-30 SCSI-50 Connectors

Pin	Function	Pin	Function
1	1553_CH1A-	26	1553_CH1A+
2	NC	27	NC
3	GND	28	GND
4	Chassis*	29	IRIG_OUT
5	IRIG_Return	30	IRIG_IN
6	NC	31	NC
7	1553_CH1B-	32	1553_CH1B+
8	NC	33	NC
9	NC	34	NC
10	GND	35	GND
11	NC	36	NC
12	~USER_LED2	37	~USER_LED1
13	1553_CH2A-	38	1553_CH2A+
14	GND	39	ADISC 2
15	RTAD0	40	ADISC 1
16	Chassis*	41	GND
17	RTAD3	42	RTAD1
18	RTAD4	43	RTAD2
19	1553_CH2B-	44	1553_CH2B+

Pin	Function
20	RTADP
21	485_NEG1
22	NC
23	NC
24	Chassis*
25	NC

Pin	Function
45	NC
46	485_POS1
47	NC
48	NC
49	NC
50	NC

NOTE

The chassis connections are tied to the R15-MPCIE Rugged 37 pin connector shell and board mounting holes and may be used as the MIL-STD-1553 shields.

A.9 RCONMPCIER Transition Cable

A.9.1 Cable Description

The cable transitions from a rugged 37 position pin connector with custom thumbscrews to 18″ flying leads. A list of the cable components is shown in the table below. A picture of the cable is shown in the figures below.

Table A-31 Transition Cable Components

Connector	Description
Rugged 37 pin	RCONMPCIER (custom Omnetics Nano-D 37 pin)

Figure A-18 RCONMPCIER

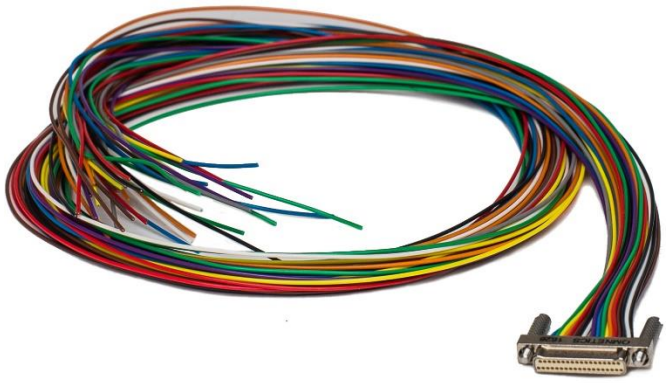
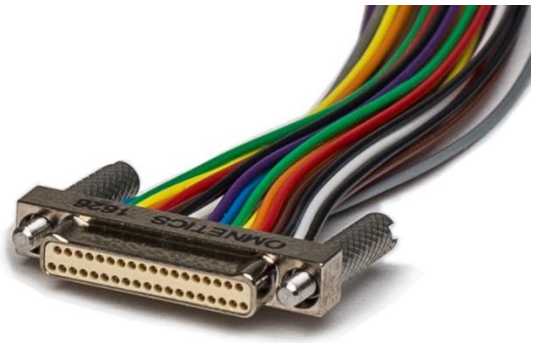


Figure A-19 RCONMPCIER Zoom



A.9.2 Transition Cable Pinouts

The table below provides the wire color for the various rugged 37 pin connector.

Table A-32 Rugged 37 Pin Connector Wire Chart

Pin #	Color
1, 11, 21, 31	Black
2, 12, 22, 32	Brown
3, 13, 23, 33	Red
4, 14, 24, 34	Orange
5, 15, 25, 35	Yellow
6, 16, 26, 36	Green
7, 17, 27, 37	Blue
8, 18, 28	Violet
9. 19. 29	Gray
10, 20, 30	White

A.10 OMNETICS A28000-037 Transition Cable

A.10.1 Cable Description

The cable transitions from a rugged 37 position pin connector with standard jack screws to 18" flying leads. This cable might allow it to fit in a tighter slot than the RCONMPCIER cable with custom thumb screws. A list of the cable components are shown in the table below. Drawings of the cable are shown in the figures below. Note that unlike in the figures below, the cable is color-coded and all the wires are individual and not tied together, similar to that shown in the RCONMPCIER cable.

Table A-33 Transition Cable Components

Connector	Description
Rugged 37 pin	Omnetics COTS A28000-037 RoHS Nano-D 37 pin

Figure A-20 A28000-037

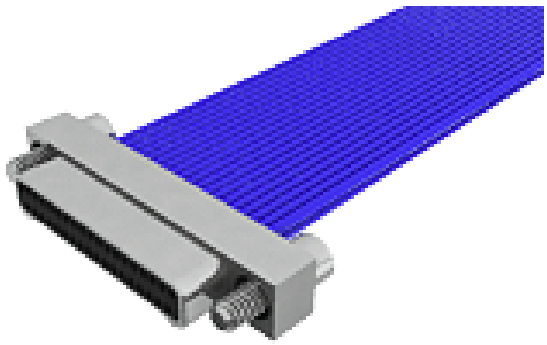
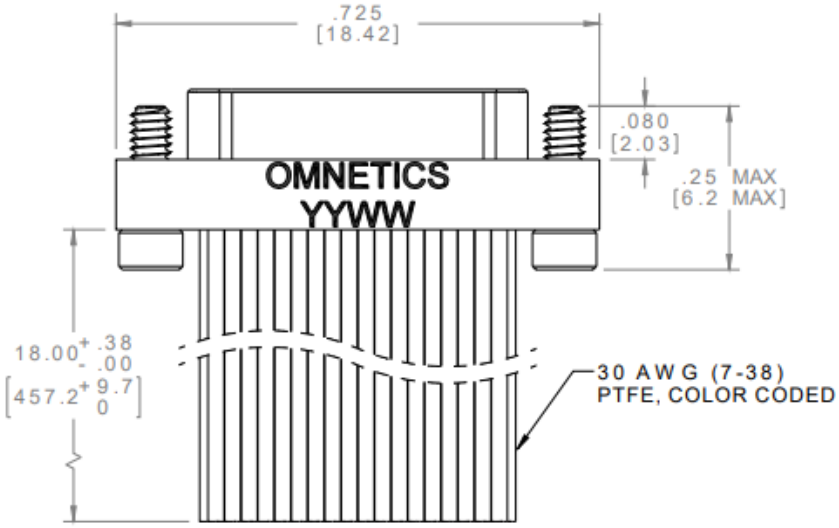


Figure A-21 A28000-037 Specification



A.10.2 Transition Cable Pinouts

The table below provides the wire color for the various rugged 37 pin connector.

Table A-34 Rugged 37 Pin Connector Wire Chart

Pin #	Color
1, 11, 21, 31	Black
2, 12, 22, 32	Brown
3, 13, 23, 33	Red
4, 14, 24, 34	Orange
5, 15, 25, 35	Yellow
6, 16, 26, 36	Green
7, 17, 27, 37	Blue
8, 18, 28	Violet
9. 19. 29	Gray
10, 20, 30	White

A.11 RCONPCCD-X Transition Cable

A.11.1 Cable Description

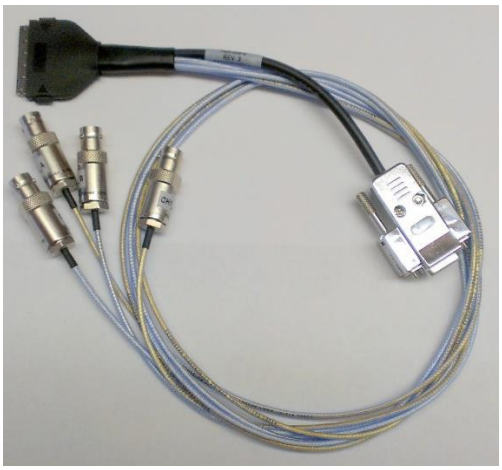
The cable transitions from a Low Profile 32 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and one D-Sub female 9 pin connector for additional I/O. A list of the cable components is shown in the table below. This cable is available in one or two channel versions where X = 1 or 2 after the dash in the product name of this Appendix section. Pictures of the cables are shown in the figures below. The nominal cable length from the back of the cards Low Profile 32 pin mating connector to the backs of the Twinax connectors is 34″. The nominal cable length from the back of the cards Low Profile 32 pin mating connector to the back of the D-Sub 9 connector 4″.

Table A-35 Transition Cable Components

Connector	Description
Low Profile 32 pin	Hirose NX30TA-32PAA(50) or equiv
D-Sub 9 pin	Tyco 5-747905-5 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-22 RCONPCCD-1

Figure A-23 RCONPCCD-2



A.11.2 Transition Cable Pinouts

The tables below provides pin assignments for the D-Sub 37 pin and 1553 Twinax connectors.

Table A-36 D-Sub 9 Pin Assignments

Pin	Signal
1	IRIGB IN
2	IRIGB_OUT
3	GND
4	TRIG IN
5	TRIG RTN [GND]
6	DISCRETE I/O 1
7	DISCRETE I/O 2
8	GND
9	TRIG OUT

Table A-37 One-channel Twinax Connectors

Connector	Signal
CH1_A	Channel 1, Bus A
CH1_B	Channel 1, Bus B

Table A-38 Two-channel Twinax Connectors

Connector	Signal
CH1_A	Channel 1, Bus A
CH1_B	Channel 1, Bus B
CH2_A	Channel 2, Bus A
CH2_B	Channel 2, Bus B

A.12 RCONRXMC2-X Transition Cable

A.12.1 Cable Description

The cable transitions from a SCSI-68 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and one D-Sub female 50 pin connector for additional I/O. A list of the cable components is shown in the table below. This cable is available in one or two channel versions where X = 2 or 4 after the dash in the product name of this Appendix section. Pictures of the cables are shown in the figures below. The nominal cable length from the back of the SCSI-68 to the backs of the Twinax connectors is 10″. The nominal cable length from the back of the SCSI-68 to the back of the D-Sub 37 is 8″.

Table A-39 Transition Cable Components

Connector	Description
SCSI-68	TE 1-5750913-7 or equiv
D-Sub 37 pin	Norcomp 171-050-202L001 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-24 RCONRXMC2-2

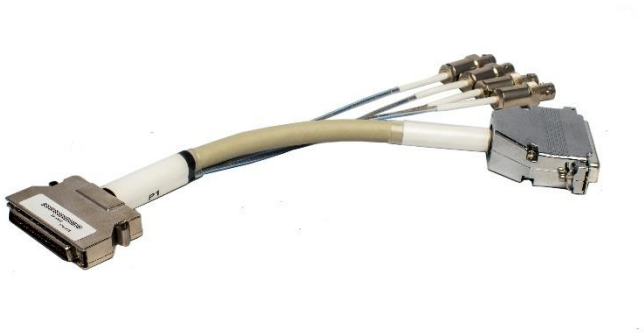


Figure A-25 RCONRXMC2-4

A.12.2 Transition Cable Pinouts

The tables below provides pin assignments for the D-Sub 50 pin and 1553 Twinax connectors.

Table A-40 D-Sub 50 Pin Assignments

Pin	Function	Pin	Function
1	DISCRETE1	26	TRIG_IN_CH4
2	DISCRETE2	27	N/C
3	GND	28	N/C
4	DISCRETE3	29	N/C
5	DISCRETE4	30	N/C
6	GND	31	N/C
7	DISCRETE5	32	N/C
8	DISCRETE6	33	N/C
9	DISCRETE7	34	EXT_TT_RST_A
10	DISCRETE8	35	EXT_TT_RST_B
11	DISCRETE9	36	N/C
12	N/C	37	N/C
13	EXT_TT_CLK_A	38	N/C
14	EXT_TT_CLK_B	39	N/C
15	N/C	40	N/C
16	N/C	41	N/C
17	N/C	42	N/C
18	DISCRETE10	43	N/C
19	DISCRETE11	44	N/C
20	DISCRETE12	45	GND
21	GND	46	IRIG_IN+
22	TRIG_IN_CH1	47	IRIG_TX
23	TRIG_IN_CH2	48	IRIG_IN-
24	TRIG_IN_CH3	49	N/C
25	GND	50	N/C

Table A-41 Two-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B

Table A-42 Four-channel Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B
J6	Channel 3, Bus A
J7	Channel 3, Bus B
J8	Channel 4, Bus A
J9	Channel 4, Bus B

A.13 R15-AMC Transition Cable

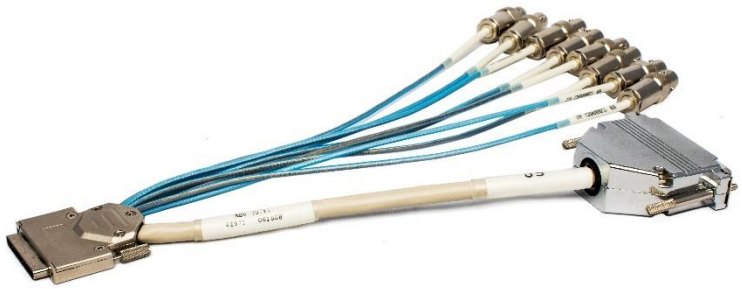
A.13.1 Cable Description

The cable transitions from a SCSI-68 pin connector to a set of male CJ70 Twinax, 3 lug, 1553 cable jacks for each available 1553 channel and one D-Sub female 50 pin connector for additional I/O. A list of the cable components is shown in the table below. This cable is available in a four channel version. Pictures of the cables are shown in the figures below. The nominal cable length from the back of the SCSI-68 to the backs of the Twinax connectors is 10″. The nominal cable length from the back of the SCSI-68 to the back of the D-Sub 50 is 8″.

Table A-43 Transition Cable Components

Connector	Description
SCSI-68	TE 1-5750913-7 or equiv
D-Sub 50 pin	Tyco 1-1218235-8 or equiv
1553 Twinax	Trompeter CJ70-49 or equiv

Figure A-26 R15-AMC Transition Cable



A.13.2 Transition Cable Pinouts

The tables below provides pin assignments for the D-Sub 50 pin and 1553 Twinax connectors.

Table A-44 J5 D-Sub 50 Pin Assignments

Pin	Signal	Pin	Signal
1	RTADDR1_0/ ADSIC 1	26	ADSIC 16
2	RTADDR1_1/ ADSIC 2	27	ADSIC 17
3	GND	28	ADSIC 18
4	RTADDR1_2/ ADSIC 3	29	GND
5	RTADDR1_3/ ADSIC 4	30	-
6	GND	31	-
7	RTADDR1_4/ ADSIC 5	32	-
8	RTADDR1_P/ ADSIC 6	33	-
9	ADSIC 7	34	-
10	ADSIC 8	35	-
11	RTADDR2_0/ ADSIC 9	36	GND
12	GND	37	-
13	EXT IN+	38	-
14	EXT IN -	39	GND
15	HWRT_EN (low true)	40	-
16	GND	41	-
17	-	42	GND
18	RTADD2_1/ ADSIC 10	43	-
19	RTADD2_2/ ADSIC 11	44	-
20	RTADD2_3/ ADSIC 12	45	GND
21	GND	46	IRIGB IN (IRIGRX_POS)
22	RTADD2_4/ ADSIC 13	47	IRIGB OUT (IRIGTX)
23	RTADD2_P/ ADSIC 14	48	IRIGB IN Return (IRIGRX_NEG)
24	ADSIC 15	49	-
25	GND	50	GND

Table A-45 Twinax Connectors

Connector	Signal
J1	Channel 1, Bus A
J2	Channel 1, Bus B
J3	Channel 2, Bus A
J4	Channel 2, Bus B
J6	Channel 3, Bus A
J7	Channel 3, Bus B
J8	Channel 4, Bus A
J9	Channel 4, Bus B

Glossary

1553	A component or message in accordance with MIL-STD-1553.
1773	A component in accordance with MIL-STD-1773, which is an optically coupled version of MIL-STD-1553.
3.x	One of several compatible versions of the Windows operating System.
32-Bit Windows®	Windows 95, 98, 98Se, Me, 2000, XP, Vista & 7.
64-Bit Windows®	Windows XP, Vista & 7.
API	Application Programmer's Interface. A defined and documented software interface, which permits software written by one person or organization to interact with the software written by another person or organization without requiring either party to know the details of the implementation of the other's software.
BC	Bus Controller. One of three possible devices that may be connected to a MIL-STD-1553 bus. Determines the message traffic on a 1553 bus.
BC-RT	A 1553 message that transfers data from the BC to a RT. Also called a RT Receive message.
BIOS	Basic Input / Output System. The resident software that initializes the computer hardware and provides low-level access to some of the computer components.
BIT	Built-In-Test.
BM	Bus Monitor. One of three possible devices that may be connected to a MIL-STD-1553 bus. A passive monitor, which cannot create or request traffic on a 1553 bus.
Broadcast	A class of 1553 messages characterized by multiple receivers and one sender. Broadcast messages are directed to the broadcast Remote Terminal number (31), but are actually received and processed by all Remote Terminals on the bus.
Broadcast BC-RT	A specific 1553 message directed to RT address 31, where all RTs receive the data sent by the BC, and that they do not respond with a status word.
Broadcast Mode Code	A class of 1553 messages, where a mode code is directed to RT address 31. This causes all RTs on the bus to process the message and not respond with a status word.
Broadcast RT-BC	A message type that is not defined or permitted on a MIL-STD-1553 bus system.

Broadcast RT-RT	A specific 1553 message, where two command words are transmitted by the BC, and that the first command word tells all RTs to listen. The second command word instructs a specific RT to ignore the listen command and to transmit data.
BSP	Board Support Package. Software used by VxWorks to setup the hardware on a specific processor board. Roughly equivalent to the BIOS on a PC.
cPCI	Compact version of the PCI interface. See PCI below.
CMC	Common Mezzanine Card, IEEE standard P1386. This is a Parent standard detailing form factor for mezzanine interface cards such as PMC.
DLL	Dynamic Link Library. A stand-alone library of software functions that may be used by an application. The DLL may be updated or changed without requiring that the application be re-compiled or re-built.
ExpressCard	A PCI Express/USB based replacement for PC Card (PCMCIA) devices. The standard defines two card widths, 34mm or 54 mm
FPGA	Field Programmable Gate Array
IP Carrier	An interface board designed to adapt one or more IP Modules to a different mechanical and electrical bus structure.
IP Module	A modular mezzanine card based on the ANSI/VITA 4-1995 (R2002) IP Module Standard. This standard was approved in 1995 and reaffirmed in 2002.
include file	A file with an extension of ".h", used by "C" programmers to contain function and data structure definitions that are shared among various program modules.
Linux	UNIX based operating system for PCs
LRU	Line Replaceable Unit. A complex component of a vehicle that can be replaced quickly.
Microcode	The instructions for the programmable element of the 1553 interface contained in the WCS.
Microsecond	1/1,000,000 (millionth) of a second. Abbreviated as μS or μSec.
Millisecond	1/1000 (thousandth) of a second. Abbreviated as ms.
MIL-STD-1553	A military communication standard that specifies the interconnection of one Bus Controller, multiple Remote Terminals and, optionally, one or more Bus Monitors, into an integrated communication system.
MIL-STD-1773	An optically coupled version of MIL-STD-1553.
Mode Code	A class of 1553 messages, using Sub Address 0 or 31 and with the word count interpreted as the mode code number. Mode codes have zero or one data word, depending on the mode code number. While all word counts are potentially valid, only a subset of the possible mode codes are valid, as specified by the standard.
NT	A Microsoft operating system, Windows NT

Operating System	Software that operates the computer such as Windows, Linux, Solaris, etc..
OS	Same as Operating System.
PC	Personal Computer.
PCI	Peripheral Component Interconnect. A board-level communication bus used in Personal Computers (and other computer systems) based on the PCI Specification from the PCI Special Interest Group.
Playback	The ability to regenerate MIL-STD-1553 message traffic on the physical bus using data that was previously recorded.
PMC	PCI Mezzanine Card, IEEE 1386.1. A slim modular mezzanine card based on the PCI specification.
RT	Remote Terminal. One of three possible devices that may be connected to a MIL-STD-1553 bus. Responds to a Bus Controller.
RT Number	The address of a specific RT. A value between 0 and 30, with 31 being reserved for the Broadcast function.
RT Receive	A 1553 message that transfers data from the Bus Controller to a Remote Terminal. Also called a BC-RT message or just a Receive message.
RT Transmit	A 1553 message that transfers data from a Remote Terminal to the Bus Controller. Also called a RT-BC message or just a Transmit message.
RT-BC	A 1553 message that transfers data from a RT to the BC. Also called a RT Transmit message.
RT-RT	A class of 1553 messages, where there are two command words transmitted by the BC. The first command tells a specific RT to listen for data, the second command word instructs another RT to transmit data. The BC is neither the source nor destination for the data.
Sub Address	The address within a RT that acts as the source or destination of a specific message. Sub Addresses 1 through 30 are used for messages, SA 0 and 31 are reserved for mode codes.
WCS	Writeable Control Store
window	A functional component of an application. A display.
Windows	One of several operating systems supplied by Microsoft corporation.
WinTel	The Windows/Intel computing platform, commonly implemented on a PC (Personal Computer).

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